3.3V/2.5V PHASE-LOCK LOOP CLOCK DRIVER ZERO DELAY BUFFER

IDT5V9352

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES OCT 28, 2014

FEATURES:

- **Phase-lock loop clock distribution for high performance clock tree applications**
- **Output enable bank control**
- **External feedback (FBIN) pin is used to synchronize the outputs to the clock input signal**
- **No external RC network required for PLL loop stability**
- **Operates at 3.3V/2.5V Vcc**
- **Spread Spectrum Compatible**
- **Operating frequency up to 200MHz**
- **Compatible with Motorola MPC9352**
- **Available in 32-pin TQFP package**
- **Use replacement part: 87952AYILF**

DESCRIPTION:

The 5V9352 is a low-skew, low-jitter, phase-lock loop (PLL) clock driver targeted for high performance clock tree applications. It uses a PLL to precisely align, in both frequency and phase. The 5V9352 operates at 2.5V and 3.3V.

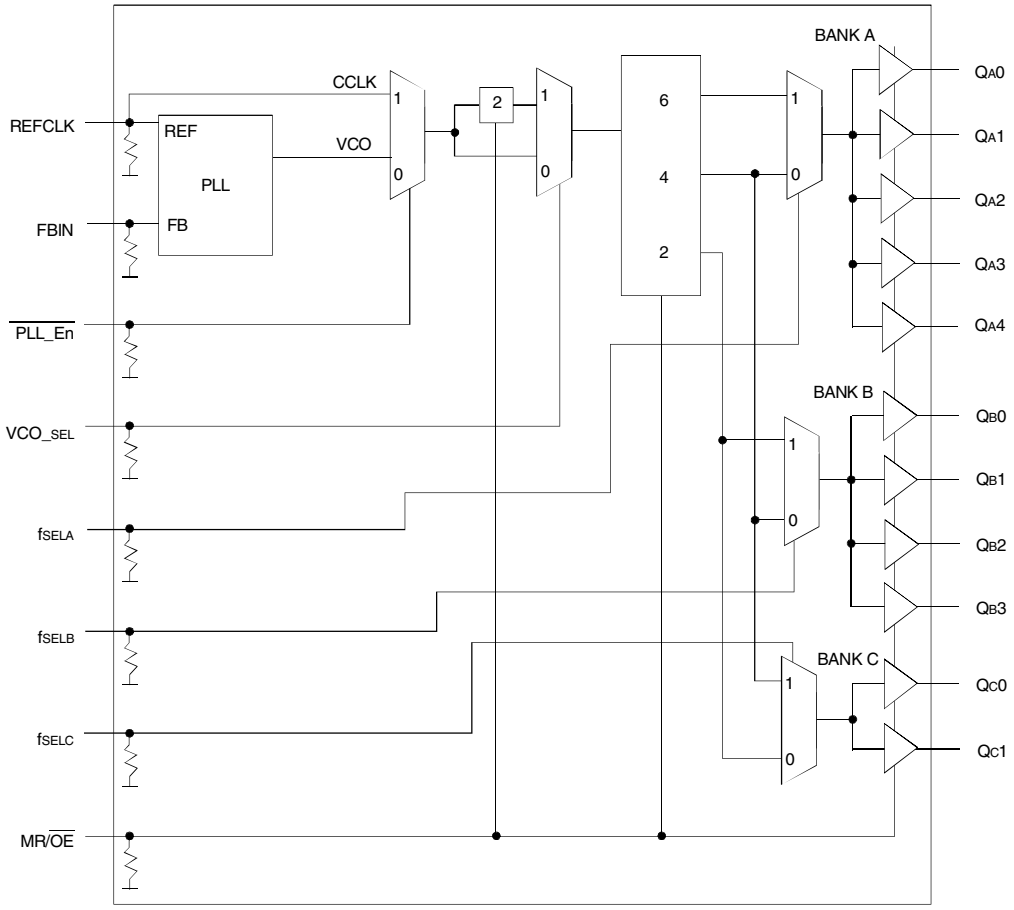
The 5V9352 features three banks of individually configurable outputs. The banks are configured with five, four, and two outputs. The internal divide circuitry allows for output frequency ratios of 1:1, 2:1, 3:1, and 3:2:1. The output frequency relationship is controlled by the fSEL frequency control pins. The fSEL pins, as well as other inputs, are LVCMOS/LVTTL compatible inputs

Unlike many products containing PLLs, the 5V9352 does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

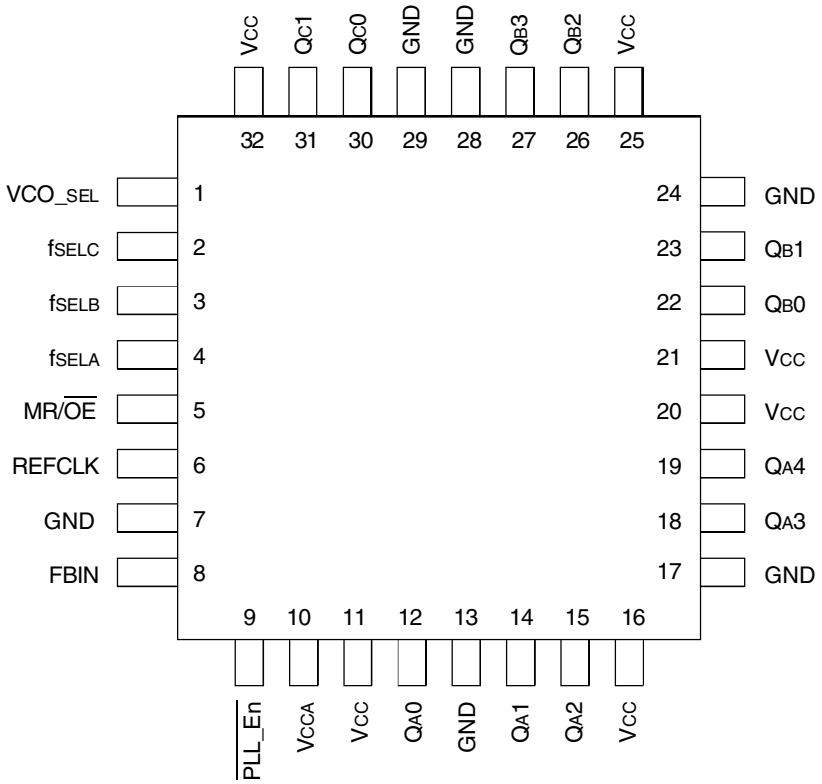
Because it is based on PLL circuitry, the 5V9352 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at REFCLK, as well as following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by setting the $\overline{\text{PLL\_EN}}$ to high.

The 5V9352 is available in Industrial temperature range (-40°C to +85°C).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TQFP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
V_{CC}	Supply Voltage Range	–0.3 to +3.6	V
V_I	Input Voltage Range	–0.3 to V_{CC}+0.3	V
I_{IN}	Input Current	±20	mA
I_{OUT}	DC Output Current	±50	mA
T_{STG}	Storage Temperature Range	–65 to +125	°C

NOTE:
1. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

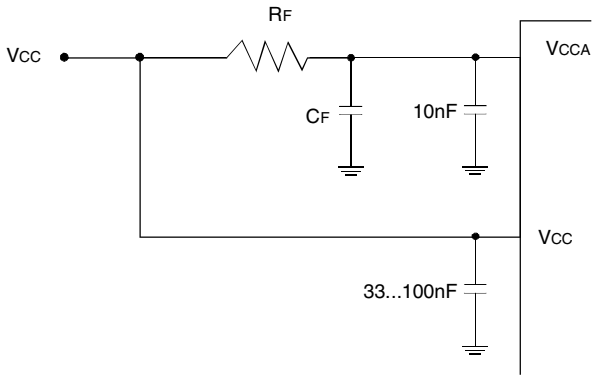
GENERAL SPECIFICATIONS

Symbol	Description	Min.	Typ.	Max.	Unit
V_{TT}	Output Termination Voltage		V_{CC}/2		V
HBM	ESD Protection (human body model)	2000			V
LU	Latch-Up Immunity	200			mA

CAPACITANCE

Parameter	Description	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	—	4	—	pF
C_{PD}	Power Dissipation Capacitance	—	10	—	pF

LOGIC DIAGRAM(1,2)



NOTES:
1. IDT5V9352 requires an external RC filter for the analog power supply pin V_{CCA}.
2. For V_{CC} = 2.5V, R_F = 9-10Ω, C_F = 22µF.
   For V_{CC} = 3.3V, R_F = 5-15Ω, C_F = 22µF.

FUNCTION TABLES

f_{SELA}	Q_{An}	f_{SELB}	Q_{Bn}	f_{SELC}	Q_{cn}
0	÷4	0	÷4	0	÷2
1	÷6	1	÷2	1	÷4

Control Pin	Logic 0	Logic 1
VCO_SEL	fVCO	fVCO / 2
MR/$\overline{OE}$	Output Enable	Outputs disable (high-impedance state) and reset of the device.
$\overline{PLL\_En}$	Enable PLL	Disable PLL

NOTE:
1. IDT5V9352 requires reset at power up and after any loss of PLL lock. Length of reset pulse should be greater than two REF CLK cycles (REFCLK).

PIN DESCRIPTION

Terminal		Type	Description
Name	No.		
REFCLK	6	I	Reference clock input
FBIN	8	I	Feedback input.
V_{CCA}	10	PWR	Analog power supply
GND	7, 13, 17, 24, 28, 29	Ground	Negative power supply
VCO_SEL	1	I	Allows for the choice of two VCO ranges to optimize PLL stability and jitter performance
MR/$\overline{OE}$	5	I	Allows the user to force the outputs into HIGH impedence for board level test
$Q_{A(0:4)}$	12, 14, 15, 18, 19	O	Clock outputs. These outputs provide low skew copies of REFCLK or can be at different frequencies than REFCLK.
$Q_{B(0:3)}$	22, 23, 26, 27		
$Q_{C(0:1)}$	30, 31		
V_{CC}	11, 16, 20, 21, 25, 32	PWR	Positive power supply for I/O and core
$\overline{PLL\_EN}$	9	I	PLL enable input. When set LOW, PLL is enabled. When set HIGH, PLL is disabled.
$f_{SEL(C:A)}$	2, 3, 4	I	Frequency control pin

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C, V_{CC} = 3.3V ± 5%

Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Level		2		V_{CC} + 0.3	V
V_{IL}	Input LOW Level				0.8	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –24mA	2.4			V
V_{OL}	LOW Level Output Voltage	I_{OL} = 12mA			0.3	V
		I_{OL} = 24mA			0.55	
Z_{OUT}	Output Impedance			14 - 17		Ω
I_I	Input Current(2)	V_I = V_{CC} or GND			±200	µA
I_{CC}	Maximum Quiescent Supply Current(3)	All V_{CC} pins			1	mA
I_{CCA}	PLL Supply Current	V_{CCA} pin		3	5	mA

NOTES:
1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. Inputs have pull-down resistors affecting the input current.
3. Icc is the DC current consumption of the device with all outputs open in high-impedance state and the inputs in its default state or open.

INPUT TIMING REQUIREMENTS

T_A = –40°C to +85°C, V_{CC} = 3.3V ± 5%

Symbol	Description		Min.	Max.	Unit
REF	Reference CLK input in PLL mode(1)	÷4 feedback	50	100	MHz
		÷6 feedback	33.3	66.6	
		÷8 feedback	25	50	
		÷12 feedback	16.67	33.3	
	Reference CLK input in PLL bypass mode(2)			250	
d_H	Input clock duty cycle		25	75	%
t_R, t_F	Maximum input rise and fall times, 0.8V to 2V		—	1	ns

NOTES:
1. PLL mode requires $\overline{PLL\_EN}$ = 0 to enable the PLL and zero delay operation.
2. In PLL bypass mode, the IDT5V9352 divides the input reference clock.

AC ELECTRICAL CHARACTERISTICS(1)

T_A = –40°C to +85°C, V_{CC} = 3.3V ± 5%

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
t_{R}, t_{F}	Output Rise/Fall Time	0.55V to 2.4V	0.1		1	ns
$t_{SK(O)}$	Output to Output Skew	All Outputs, any frequency			200	ps
		within Q_A output bank			200	
		within Q_B output bank			100	
		within Q_C output bank			100	
f_{VCO}	PLL VCO Lock Range(2)		200		400	MHz
f_{MAX}	Maximum Output Frequency	÷2 output	100		200	MHz
		÷4 output	50		100	
		÷6 output	33.3		66.6	
		÷8 output	25		50	
		÷12 output	16.67		33.3	
t_{PW}	Output Duty Cycle		47	50	53	%
t_{PD}	REFCLK to FBIN Delay	f_{REF} < 40MHz	-200		+150	ps
	PLL Locked	f_{REF} > 40MHz, PLL locked	-50		+150	
t_{PLZ} t_{PHZ}	Output Disable Time MR/$\overline{OE}$ (LOW-HIGH) to any Q				8	ns
t_{PZL} t_{PZH}	Output Enable Time MR/$\overline{OE}$ (HIGH-LOW) to any Q				10	ns
t_J	Cycle-to-Cycle Jitter	Output frequencies mixed			400	ps
		Outputs in any ÷4 and ÷6 combination			250	
		All outputs same frequency			100	
$t_{J(PER)}$	Period Jitter	Output frequencies mixed			200	ps
		Outputs in any ÷4 and ÷6 combination			150	
		All outputs same frequency			75	
$t_{J(\phi)}$	I/O Phase Jitter	÷4 feedback divider RMS (1σ)		15		ps
		÷6 feedback divider RMS (1σ)		20		
		÷8 feedback divider RMS (1σ)		18-20		
		÷12 feedback divider RMS (1σ)		25		
BW	PLL Closed Loop Bandwidth	÷4 feedback		3 - 10		MHz
		÷6 feedback		1.5 - 6		
		÷8 feedback		1 - 3.5		
		÷12 feedback		0.5 - 2		
t_{LOCK}	Maximum PLL Lock Time				10	ms

NOTES:

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The input frequency on CCLK must match the VCO frequency range divided by the feedback divide ratio FB: freq. = fvco ÷ FB.

DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C, V_{CC} = 2.5V ± 5%

Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Level	LVCMOS	1.7		V_{CC} + 0.3	V
V_{IL}	Input LOW Level	LVCMOS	–0.3		0.7	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = –15mA	1.8			V
V_{OL}	LOW Level Output Voltage	I_{OL} = 15mA			0.6	V
Z_{OUT}	Output Impedance			17 - 20		Ω
I_I(2)	Input Current	V_I = V_{CC} or GND			±200	µA
I_{CC}(3)	Maximum Quiescent Supply Current				1	mA
I_{CCA}	PLL Supply Current			2	5	mA

NOTES:
1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. Inputs have pull-down resistors affecting the input current.
3. Icc is the DC current consumption of the device with all outputs open in High-Impedance state and the inputs in its default state (or open).

INPUT TIMING REQUIREMENTS

T_A = –40°C to +85°C, V_{CC} = 2.5V ± 5%

Symbol	Description		Min.	Max.	Unit
REF	Reference CLK input(1)	÷4 feedback	50	100	MHz
		÷6 feedback	33.3	66.6	
		÷8 feedback	25	50	
		÷12 feedback	16.67	33.3	
	Reference CLK input in PLL bypass mode(2)			250	
d_H	Input clock duty cycle		25	75	%
t_R, t_F	Maximum input rise and fall times, 0.8V to 2V		——	1	ns

NOTES:
1. Maximum and minimum input reference is limited by the VCO clock range and the feedback divider.
2. In PLL bypass mode, the 5V9352 divides the input reference clock.

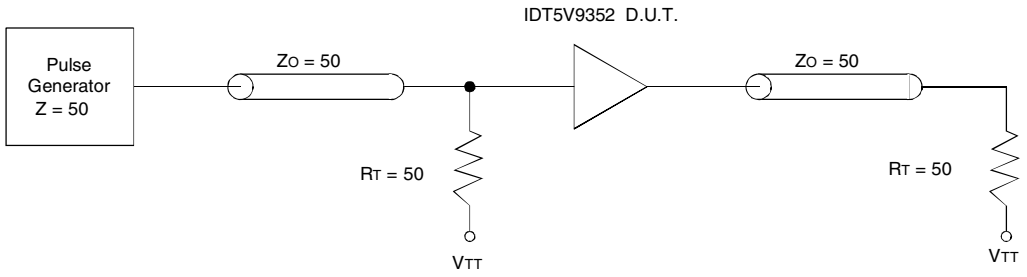
AC ELECTRICAL CHARACTERISTICS(1)

T_A = –40°C to +85°C, V_{CC} = 2.5V ± 5%

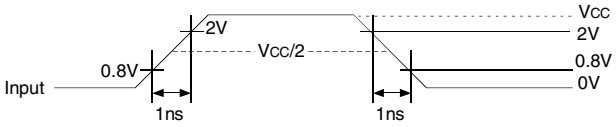
Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
t_{R}, t_{F}	Output Rise/Fall Time	0.6V to 1.8V	0.1		1	ns
$t_{SK(O)}$	Output to Output Skew	All Outputs, any frequency			200	ps
		within Q_A output bank			200	
		within Q_B output bank			100	
		within Q_C output bank			100	
f_{VCO}	PLL VCO Lock Range		200		400	MHz
f_{MAX}	Maximum Output Frequency	÷2 output	100		200	MHz
		÷4 output	50		100	
		÷6 output	33.3		66.6	
		÷8 output	25		50	
		÷12 output	16.67		33.3	
t_{PW}	Output Duty Cycle		47	50	53	%
t_{PD}	REFCLK to FBIN Delay	f_{REF} < 40MHz	-200		+150	ps
	PLL Locked	f_{REF} > 40MHz	-50		+150	
t_{PLZ} t_{PHZ}	Output Disable Time MR/$\overline{OE}$ (LOW-HIGH) to any Q				8	ns
t_{PZL} t_{PZH}	Output Enable Time MR/$\overline{OE}$ (HIGH-LOW) to any Q				10	ns
t_J	Cycle-to-Cycle Jitter	Output frequencies mixed			400	ps
		Outputs in any ÷4 and ÷6 combination			250	
		All outputs same frequency			100	
$t_{J(PER)}$	Period Jitter	Output frequencies mixed			200	ps
		Outputs in any ÷4 and ÷6 combination			150	
		All outputs same frequency			75	
$t_{J(\phi)}$	I/O Phase Jitter	÷4 feedback divider RMS (1σ)		15		ps
		÷6 feedback divider RMS (1σ)		20		
		÷8 feedback divider RMS (1σ)		18-20		
		÷12 feedback divider RMS (1σ)		25		
BW	PLL Closed Loop Bandwidth	÷4 feedback		1 - 8		MHz
		÷6 feedback		0.7 - 3		
		÷8 feedback		0.5 - 2.5		
		÷12 feedback		0.4 - 1		
t_{LOCK}	Maximum PLL Lock Time				10	ms

NOTE:
1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

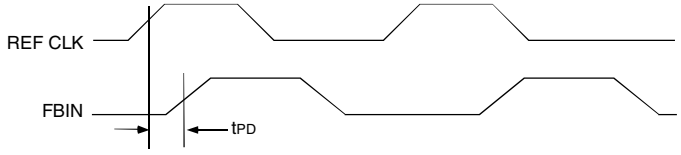
TEST CIRCUITS AND WAVEFORMS



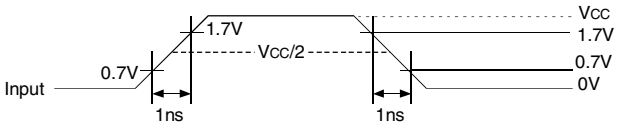
AC Test Reference for Vcc = 2.5V and Vcc = 3.3V



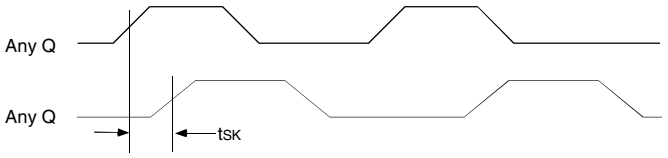
Input Characteristics for 3.3V



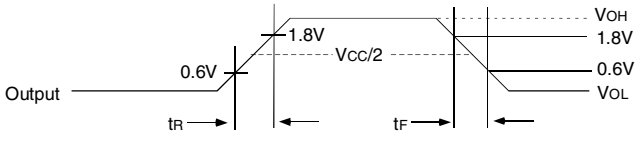
Prop Delay



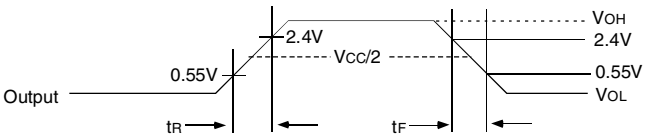
Input Characteristics for 2.5V



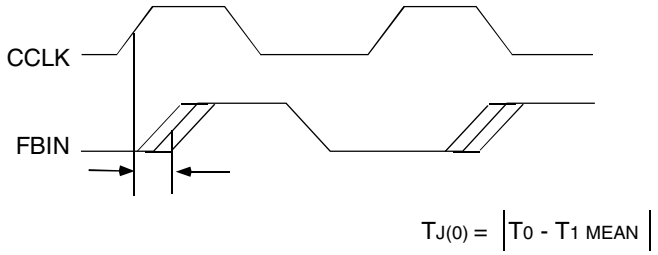
Skew Calculations



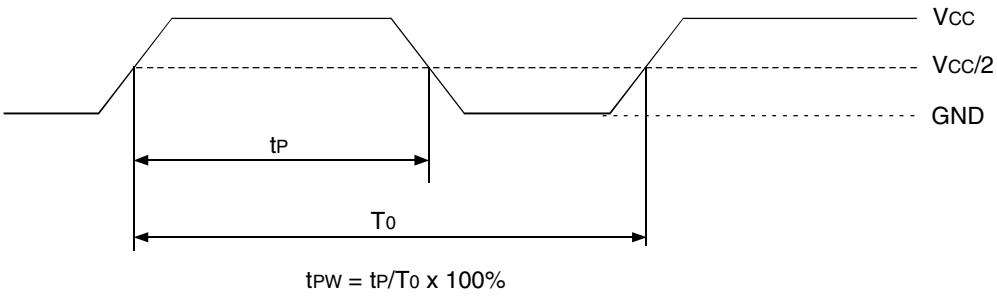
Output Test Conditions for Vcc = 2.5V ± 5%



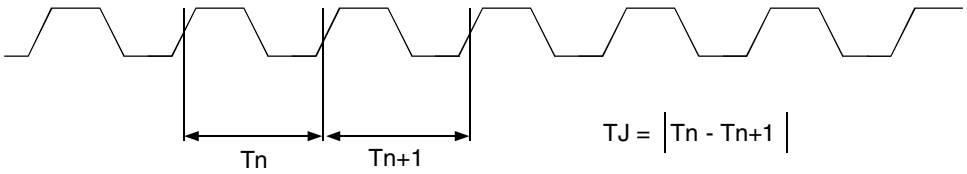
Output Test Conditions for Vcc = 3.3V ± 5%



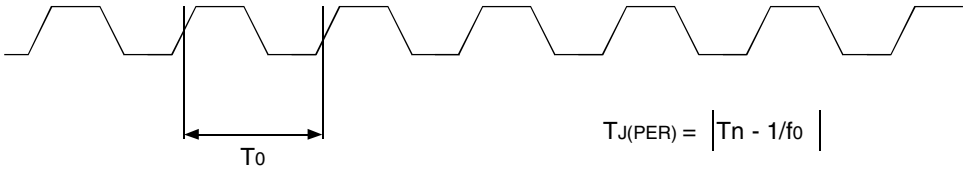
I/O Jitter



Output Duty Cycle

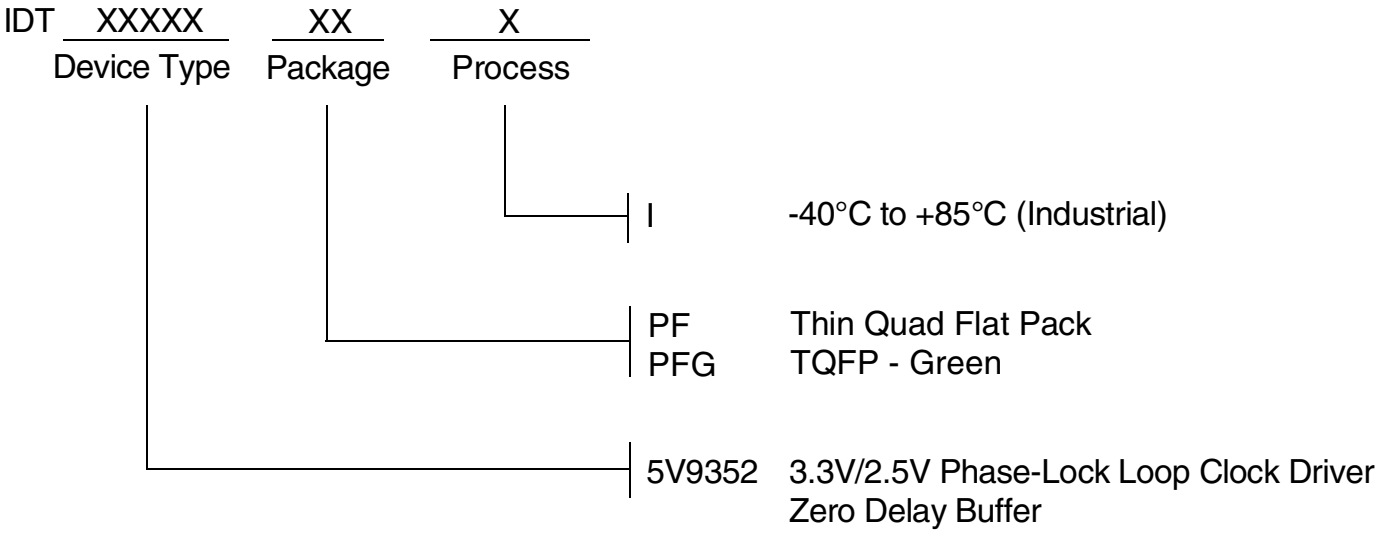


Cycle-to-Cycle Jitter



Period Jitter

ORDERING INFORMATION



REVISION HISTORY

Rev	Table	Page	Discription of Change	Date
A		1	NRND - Not Recommended for New Designs	5/20/13
A		1	PDN - Product Discontinuation Notice - Last Time Buy Expires October 28, 2014 - PDN# CQ-13-02	12/19/13

We've Got Your Timing Solution.

www.IDT.com

6024 Silver Creek Valley Road
San Jose, CA 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Tech Support
netcom@idt.com
+480-763-2056