MAX7304
I2C-Interfaced 16-Port, Level-Translating GPIO and LED Driver with High Level of Integrated ESD Protection

General Description

The MAX7304 consists of 16 port GPIOs, with 12 push-pull GPIOs and four open-drain GPIOs configurable as PWM-controlled LED drivers. The device supports a 1.62V to 3.6V separate power supply for level translation. An address-select input (AD0) allows up to four unique slave addresses for the device.

Each GPIO can be programmed to one of the two externally applied logic voltage levels. PORT15–PORT12 can also be configured as LED drivers that feature constant-current sinks and PWM intensity control with the internal oscillator. The maximum constant-current level for each open-drain LED port is 20mA. The intensity of the LED on each open-drain port can be individually adjusted through a 256-step PWM control. The port also features LED fading.

The same index rows and columns in the device can be used as a direct logic-level translator.

The device is offered in a 24-pin (3.5mm x 3.5mm) TQFN package with an exposed pad, and a small 25-bump (2.159mm x 2.159mm) wafer-level package (WLP) for cell phones, pocket PCs, and other portable consumer electronic applications.

The device operates over the -40°C to +85°C extended temperature range.

Applications

Cell Phones

Notebooks

PDAs

Handheld Games

Portable Consumer Electronics

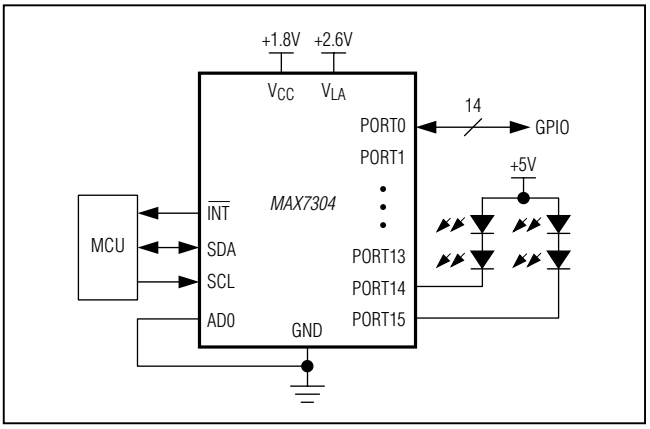
Features

- **Four LED Driver Pins on PORT15–PORT12**
- **Integrated High-ESD Protection**
  - **±8kV IEC 61000-4-2 Contact Discharge**
  - **±15kV IEC 61000-4-2 Air-Gap Discharge**
- **5V Tolerant, Open-Drain I/O Ports Capable of Constant-Current LED Drive**
- **256-Step PWM Individual LED Intensity-Control Accuracy**
- **Individual LED Blink Rates and Common LED Fade-In/Out Rates from 256ms to 4096ms**
- **User-Configurable Debounce Time (1ms to 32ms)**
- **Configurable Edge-Triggered Port Interrupt ($\overline{INT}$)**
- **1.62V to 3.6V Operating Supply Voltage**
- **Individually Programmable GPIOs to Two Logic Levels**
- **8-Channel Individual Programmable Level Translators**
- **Supports Hot Insertion**
- **400kbps, 5.5V Tolerant I²C Serial Interface with Selectable Bus Timeout**

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX7304.related**.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5949; Rev 2; 5/15

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{LA} to GND .....-0.3V to +4V
PORT11–PORT0 to GND..... -0.3V to (V_{CC} + 0.3V)
PORT15–PORT12 to GND.....-0.3V to +6V
SDA, SCL, AD0, $\overline{INT}$ to GND .....-0.3V to +6V
V_{LA} to V_{CC} .....-0.3V to +2.3V
DC Current on PORT15–PORT12 to GND 25mA
DC Current on PORT11–PORT0 to GND 7mA
V_{CC}, V_{LA}, GND Current 80mA
DC Current V_{CC}, V_{LA} to PORT11–PORT0 .....5mA

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 15.4mW/°C above +70°C).....1229mW
WLP (derate 19.2mW/°C above +70°C).....850mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (TQFN) (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA})....65.1°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....5.4°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....52°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 1.62V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{CC}			1.62	3.3	3.6	V
Second Logic Supply	V_{LA}			V_{CC}	3.3	3.6	V
Operating Supply Current	I_{CC}	Oscillator running			50	65	µA
Sleep-Mode Supply Current	I_{SL}	Not using GPO or LED configuration			1.8	3	µA
POR Threshold	V_{POR}				1.2		V
GPIO SPECIFICATIONS							
External Supply Voltage PORT15–PORT12 (LED Drivers)	V_{LED}					5	V
LED Port-to-Port Sink Current Variation		V_{CC} = 3.3V, V_{OL} = 1V, T_A = +25°C, 10mA output mode			±1.5	±2.4	%
10mA Port Sink Current PORT15–PORT12	I_{OL}	V_{OL} = 1V	T_A = +25°C	8.6		11.4	mA
			V_{CC} = 3.3V	9.04	10	10.96	
		V_{OL} = 0.5V	V_{CC} = 3.6V, T_A = +25°C		9.5		
20mA Port Sink Current PORT15–PORT12	I_{OL}	V_{OL} = 1V	T_A = +25°C	18.13		21.52	mA
			V_{CC} = 3.3V	18.47	20	21.34	
		V_{OL} = 0.5V	V_{CC} = 3.6V, T_A = +25°C		19.05		
Input High Voltage PORT_	V_{IH}	V_S = V_{CC} or V_{LA} depending on reference logic level setting		0.7 x V_S			V
Input Low Voltage PORT_	V_{IL}					0.3 x V_S	V
Input Leakage Current PORT11–PORT0	$I_{LEAKAGE}$	Input voltage = V_{CC} or V_{GND}		-2		+2	µA
Input Leakage Current PORT15–PORT12	$I_{LEAKAGE}$	Input voltage = 5V		-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.62V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance PORT_	C_{IN}			20		pF
Output Low Voltage PORT_	V_{OL}	V_{CC} = 1.62V and I_{SINK} = 2.5mA		50	100	mV
		V_{CC} = 1.62V and I_{SINK} = 5mA		80	250	
Output High Voltage COL3–COL0, ROW_	V_{OH}	V_{CC} = 1.62V and I_{SOURCE} = 2.5mA	V_{CC} - 120	V_{CC} - 40		mV
		V_{CC} = 1.62V and I_{SOURCE} = 5mA	V_{CC} - 250	V_{CC} - 70		
Output Logic-Low Voltage ($\overline{INT}$)	V_{OL}	I_{SINK} = 6mA			0.6	V
PWM Frequency	f_{PWM}	Derived from oscillator clock		500		Hz
SERIAL-INTERFACE SPECIFICATIONS						
Input High Voltage SDA, SCL, AD0	V_{IH}		0.7 x V_{CC}			V
Input Low Voltage SDA, SCL, AD0	V_{IL}				0.3 x V_{CC}	V
Input Leakage Current SDA, SCL, AD0	$I_{LEAKAGE}$	Input voltage = 5.5V or V_{GND}	-1		+1	µA
Output Logic-Low Voltage SDA	V_{OL}	I_{SINK} = 6mA			0.6	V
Input Capacitance SDA, SCL, AD0	C_{IN}	(Notes 4, 5)			10	pF
I²C TIMING SPECIFICATIONS						
SCL Serial-Clock Frequency	f_{SCL}	Bus timeout enabled	0.05		400	kHz
		Bus timeout disabled	0		400	
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 6)			0.9	µs
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 4, 5)		20 + 0.1C_B	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 4, 5)		20 + 0.1C_B	300	ns
Fall Time of SDA Signal, Transmitting	$t_{F, TX}$	(Notes 4, 7)		20 + 0.1C_B	250	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 1.62V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Notes 2, 3)

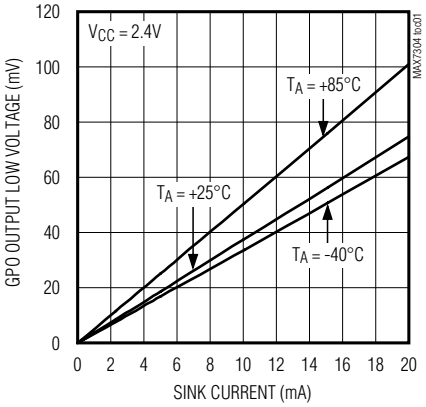
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pulse Width of Spike Suppressed	t_{SP}	(Notes 4, 8)			50	ns
Capacitive Load for Each Bus Line	C_B	(Note 4)			400	pF
Bus Timeout	$t_{TIMEOUT}$		14	19	27	ms
ESD PROTECTION						
PORT_		IEC 61000-4-2 Air-Gap Discharge		±15		kV
		IEC 61000-4-2 Contact Discharge		±8		
All Other Pins		Human Body Model		±2.5		kV

Note 2: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: All digital inputs at V_{CC} or GND.
Note 4: Guaranteed by design.
Note 5: C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.
Note 6: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.
Note 7: I_{SINK} = 6mA. C_B = total capacitance of one bus line in pF. t_R and t_F measured between 0.8V and 2.1V.
Note 8: Input filters on the SDA, SCL, and AD0 inputs suppress noise spikes less than 50ns.

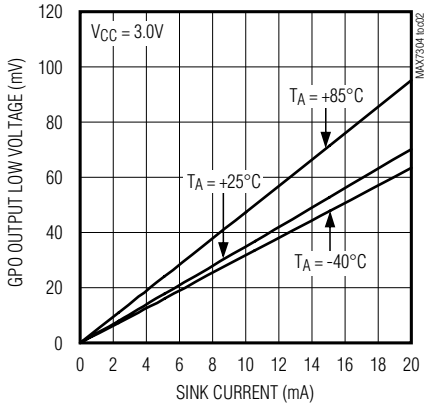
Typical Operating Characteristics

(V_{CC} = 2.5V, V_{LA} = 2.5V, T_A = +25°C, unless otherwise noted.)

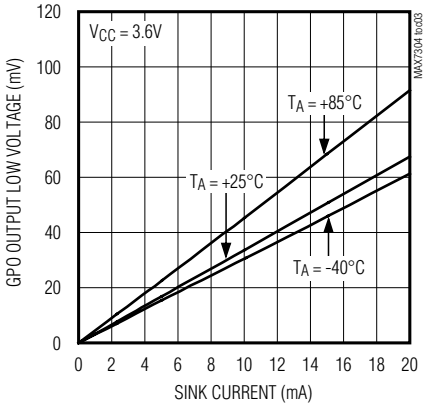
GPO OUTPUT LOW VOLTAGE vs. SINK CURRENT (PORT15–PORT12)



GPO OUTPUT LOW VOLTAGE vs. SINK CURRENT (PORT15–PORT12)



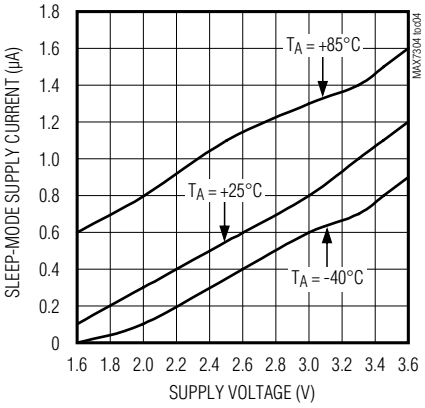
GPO OUTPUT LOW VOLTAGE vs. SINK CURRENT (PORT15–PORT12)



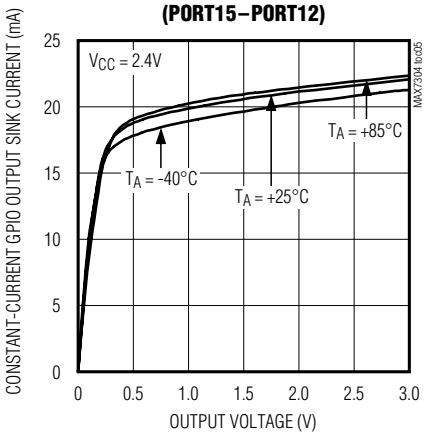
Typical Operating Characteristics (continued)

(V_{CC} = 2.5V, V_{LA} = 2.5V, T_A = +25°C, unless otherwise noted.)

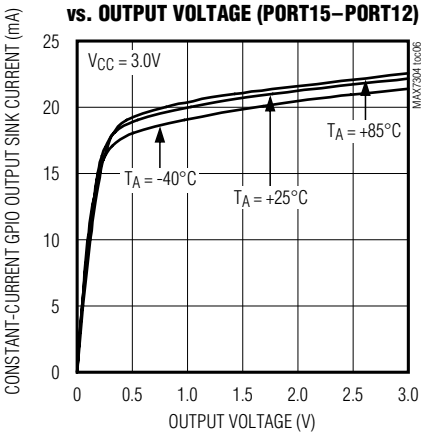
SLEEP-MODE SUPPLY CURRENT vs. SUPPLY VOLTAGE



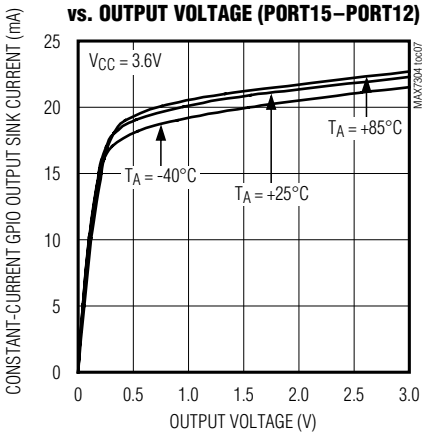
CONSTANT-CURRENT GPIO OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (PORT15–PORT12)



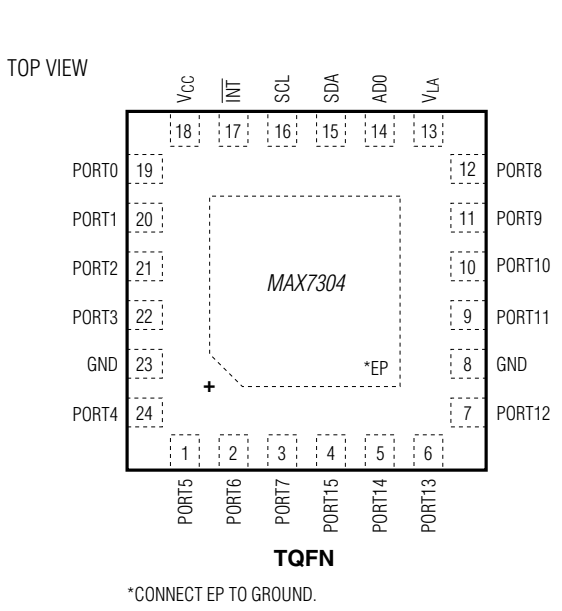
CONSTANT-CURRENT GPIO OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (PORT15–PORT12)



CONSTANT-CURRENT GPIO OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE (PORT15–PORT12)

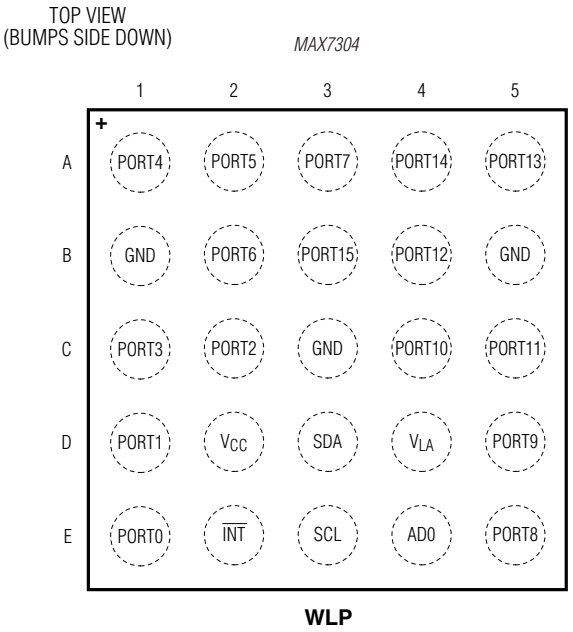


Pin/Bump Configurations



TQFN

*CONNECT EP TO GROUND.



WLP

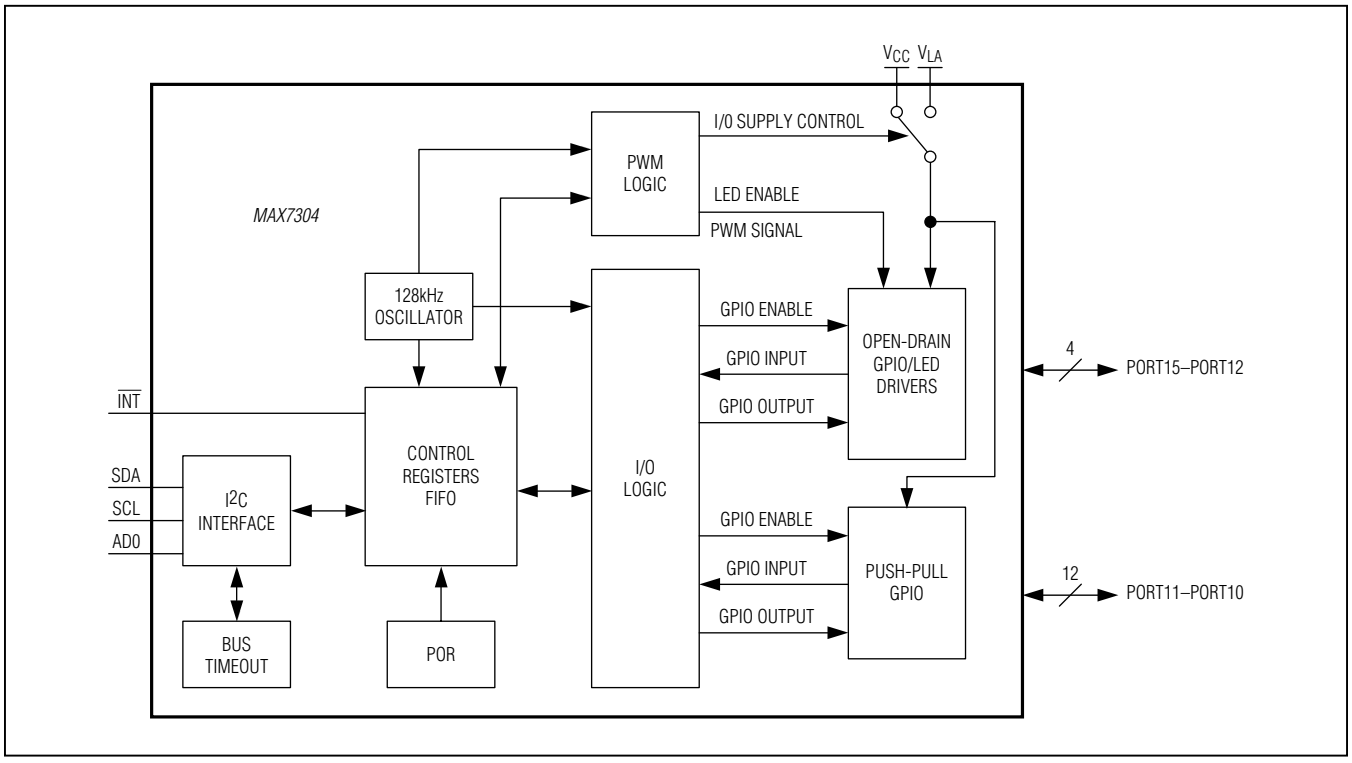
Pin/Bump Description

PIN	BUMP	NAME	FUNCTION
TQFN	WLP		
1	A2	PORT5	GPIO Port 5. Push-pull I/O.
2	B2	PORT6	GPIO Port 6. Push-pull I/O.
3	A3	PORT7	GPIO Port 7. Push-pull I/O.
4	B3	PORT15	GPIO Port 15. Open-drain I/O. PORT15 can be configured as a constant-current sink.
5	A4	PORT14	GPIO Port 14. Open-drain I/O. PORT14 can be configured as a constant-current sink.
6	A5	PORT13	GPIO Port 13. Open-drain I/O. PORT13 can be configured as a constant-current sink.
7	B4	PORT12	GPIO Port 12. Open-drain I/O. PORT12 can be configured as a constant-current sink.
8, 23	B1, B5, C3	GND	Ground
9	C5	PORT11	GPIO Port 11. Push-pull I/O.
10	C4	PORT10	GPIO Port 10. Push-pull I/O.
11	D5	PORT9	GPIO Port 9. Push-pull I/O.
12	E5	PORT8	GPIO Port 8. Push-pull I/O.
13	D4	V_{LA}	Second Logic Level for GPIO Level Shifting (where $V_{CC} \le V_{LA} \le 3.6V$)
14	E4	AD0	Address Input. Selects up to four device slave addresses (Table 2).
15	D3	SDA	I²C-Compatible, Serial-Data I/O
16	E3	SCL	I²C-Compatible Serial-Clock Input
17	E2	$\overline{INT}$	Active-Low Key-Switch Interrupt Output. $\overline{INT}$ is open-drain and requires a pullup resistor.

Pin Description (continued)

PIN TQFN	BUMP WLP	NAME	FUNCTION
18	D2	V_{CC}	Positive Supply Voltage. Bypass to GND with a 0.1µF capacitor as close as possible to the device.
19	E1	PORT0	GPIO Port 0. Push-pull I/O.
20	D1	PORT1	GPIO Port 1. Push-pull I/O.
21	C2	PORT2	GPIO Port 2. Push-pull I/O.
22	C1	PORT3	GPIO Port 3. Push-pull I/O.
24	A1	PORT4	GPIO Port 4. Push-pull I/O.
—	—	EP	Exposed Pad (TQFN Only). Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Functional Diagram



Detailed Description

The MAX7304 is an I²C-interfaced 16-port GPIO expander. The device features 12 push-pull GPIOs configured for digital I/O and four open-drain GPIOs configurable as constant-current outputs for LED applications up to 5V. The device supports a second 1.62V to 3.6V power supply for level translation. The second logic supply voltage (V_{LA}) must be set equal to or higher than V_{CC}.

Each GPIO can be programmed to one of the two externally applied logic voltage levels. PORT15–PORT12 can also be configured as LED drivers that feature constant-current and PWM intensity control. The maximum constant-current level for each open-drain LED port is 20mA. The intensity of the LED on each open-drain port can be individually adjusted through a 256-step PWM control. The port also features LED fading.

The device meets ESD requirements for ±8kV contact discharge and ±15kV air-gap discharge on all port pins (configured as GPIO and/or LED drivers).

Initial Power-Up

On power-up, all control registers reset to power-up values (Table 1) and the device is in sleep mode.

Table 1. Register Address Map and Power-Up Conditions

ADDRESS CODE (hex)	READ/ WRITE	POWER-UP VALUE (hex)	REGISTER FUNCTION	DESCRIPTION
0x01	R/$\overline{W}$	0x0B	Configuration	Power-down and I²C timeout enable
0x31	R/$\overline{W}$	0x00	LED driver enable	LED driver enable register
0x32	R/$\overline{W}$	0xFF	GPI enable	GPI enable for PORT7–PORT0
0x33	R/$\overline{W}$	0xFF	GPI enable	GPI enable for PORT15–PORT8
0x34	R/$\overline{W}$	0x00	GPIO direction 1	GPIO input/output control register 1 for PORT7–PORT0
0x35	R/$\overline{W}$	0x00	GPIO direction 2	GPIO input/output control register 2 for PORT15–PORT8
0x36	R/$\overline{W}$	0xFF	GPO output mode 1	GPO open-drain/push-pull output setting for PORT7–PORT0
0x37	R/$\overline{W}$	0x0F	GPO output mode 2	GPO open-drain/push-pull output setting for PORT15–PORT8
0x38	R/$\overline{W}$	0x00	GPIO supply voltage 1	GPIO voltages supplied by V_{CC} or V_{LA} for PORT7–PORT0
0x39	R/$\overline{W}$	0x00	GPIO supply voltage 2	GPIO voltages supplied by V_{CC} or V_{LA} for PORT15–PORT8
0x3A	R/$\overline{W}$	0xFF	GPIO values 1	Debounced input or output values of PORT7–PORT0
0x3B	R/$\overline{W}$	0xFF	GPIO values 2	Debounced input or output values of PORT15–PORT8
0x3C	R/$\overline{W}$	0x00	GPIO level-shifter enable	GPIO level-shifter pair enable
0x40	R/$\overline{W}$	0x00	GPIO global configuration	GPIO standby, GPIO reset, LED fade
0x42	R/$\overline{W}$	0x00	GPIO debounce	PORT7–PORT0 debounce time setting
0x43	R/$\overline{W}$	0xC0	LED constant-current setting	PORT15–PORT12 constant-current output setting
0x45	R/$\overline{W}$	0x00	Common PWM	Common PWM duty-cycle setting
0x48	Read only	0x00	I²C timeout flag	I²C timeout since last POR
0x50	R/$\overline{W}$	0x00	PORT12 PWM ratio	PORT12 individual duty-cycle setting
0x51	R/$\overline{W}$	0x00	PORT13 PWM ratio	PORT13 individual duty-cycle setting
0x52	R/$\overline{W}$	0x00	PORT14 PWM ratio	PORT14 individual duty-cycle setting
0x53	R/$\overline{W}$	0x00	PORT15 PWM ratio	PORT15 individual duty-cycle setting

Table 1. Register Address Map and Power-Up Conditions (continued)

ADDRESS CODE (hex)	READ/ WRITE	POWER-UP VALUE (hex)	REGISTER FUNCTION	DESCRIPTION
0x54	R/$\overline{W}$	0x00	PORT12 LED configuration	PORT12 interrupt, PWM mode control, and blink-period settings
0x55	R/$\overline{W}$	0x00	PORT13 LED configuration	PORT13 interrupt, PWM mode control, and blink-period settings
0x56	R/$\overline{W}$	0x00	PORT14 LED configuration	PORT14 interrupt, PWM mode control, and blink-period settings
0x57	R/$\overline{W}$	0x00	PORT15 LED configuration	PORT15 interrupt, PWM mode control, and blink-period settings
0x58	R/$\overline{W}$	0xFF	Interrupt mask 1	Interrupt mask for PORT7–PORT0
0x59	R/$\overline{W}$	0xFF	Interrupt mask 2	Interrupt mask for PORT15–PORT8
0x5A	R/$\overline{W}$	0x00	GPI trigger mode 1	GPI edge-triggered detection setting for PORT7–PORT0
0x5B	R/$\overline{W}$	0x00	GPI trigger mode 2	GPI edge-triggered detection setting for PORT15–PORT8

GPIOs

The device has 16 GPIO ports, of which four have LED control functions. The ports can be used as logic inputs and logic outputs. PORT15–PORT12 are also configurable as constant-current PWM LED drivers. Each ports' logic level is referenced to V_{CC} or V_{LA}. The GPIO port's inputs can also be debounced. When in PWM mode, the ports are set up to start their PWM cycle in 45° phase increments. This prevents large current spikes on the LED supply voltage when driving multiple LEDs.

Configuration Register (0x01)

The configuration register controls the I²C bus timeout feature (see Table 5 in the *Register Tables* section). The bus timeout feature prevents the SDA being held low when the SCL line hangs.

LED Driver Enable Register (0x31)

Bits D[3:0] correspond to PORT15–PORT12 on the device. Set the corresponding bit to 1 for enabling the LED driver circuitry and 0 for normal GPIO function (see Table 6 in the *Register Tables* section).

GPIO Direction 1 and 2 Registers (0x34, 0x35)

These registers configure the pin as an input or an output. GPIO direction 1 register bits D[7:0] correspond with PORT7–PORT0 (see Table 7 in the *Register Tables* section). GPIO direction 2 register bits D[7:0] correspond with PORT15–PORT8 (see Table 8 in the *Register Tables* section). Set the corresponding bit to 0 to configure as input and 1 to configure as output.

When the port is initially programmed as an input, there is a delay of one debounce period prior to detecting a transition on the input port. This is to prevent a false interrupt from occurring when changing a port from an output to an input.

GPO Output Mode 1 and 2 Registers (0x36, 0x37)

These registers configure the pins as an open-drain or push-pull output. GPO output mode 1 register bits D[7:0] correspond with PORT7–PORT0 (see Table 9 in the *Register Tables* section). GPO output mode 2 register bits D[7:0] correspond with PORT15–PORT8 (see Table 10 in the *Register Tables* section). Set the corresponding bit to 0 to configure the output mode as open-drain and 1 to configure the output mode as push-pull.

GPIO Supply Voltage 1 and 2 Registers (0x38, 0x39)

These registers configure input and output voltages to be referenced to V_{CC} or V_{LA}. GPIO supply voltage 1 register bits D[7:0] correspond with PORT7–PORT0 (see Table 11 in the *Register Tables* section). GPIO supply voltage 2 register bits D[7:0] correspond with PORT15–PORT8 (see Table 12 in the *Register Tables* section). Set the bit to 0 for input/output voltages referenced to V_{CC} and set the bit to 1 for the input/output voltage referenced to V_{LA}.

GPIO Values 1 and 2 Registers (0x3A, 0x3B)

The GPIO values 1 and 2 registers contain the debounced input data for all the GPIOs for PORT7–PORT0 and PORT15–PORT8, respectively (see Tables 13 and 14 in the *Register Tables* section). There is one debounce period delay prior to detecting a transition on the input port. This prevents a false interrupt from occurring when changing a port from an output to an input. The GPIO values 1 and 2 registers reports the state of all input ports regardless of any interrupt mask settings.

When writing to the GPIO values 1 and 2 registers, the corresponding PORT_ voltage is set high when written 1 or cleared when written 0. Reading the port when configured as an output always returns the value 0 for the corresponding port regardless of the output value.

GPIO Level-Shifter Enable Register (0x3C)

Enabling bit D_ in this register enables the direct level shifter between GPIO pins PORT15–PORT8 and PORT7–PORT0 (see Table 15 in the *Register Tables* section). The level-shifting pairs are PORT0/PORT8, PORT1/PORT9, etc. The direction of the level shifter is controlled by the GPIO direction 2 register (0x35). When the corresponding bit in the GPIO direction 2 register is set to 0, PORT15–PORT8 are inputs, while PORT7–PORT0 are outputs. When the bit is set to 1, PORT7–PORT0 are inputs, while PORT15–PORT8 are outputs.

GPIO Global Configuration Register (0x40)

The GPIO global configuration register controls the main settings for the GPIO ports (see Table 16 in the *Register Tables* section).

Bit D5 enables interrupt generation for I²C timeouts. D4 is the main enable/shutdown bit for the GPIOs. Bit D3 functions as a software reset for the GPIO registers (0x31 to 0x5B). Bits D[2:0] set the fade-in/out time for the GPIOs configured as constant-current sinks.

GPIO Debounce Configuration Register (0x42)

The GPIO debounce configuration register sets the amount of time a GPIO must be held in order for the device to register a logic transition (see Table 17 in the *Register Tables* section). Five bits (D[4:0]) set 32 possible debounce times from 9ms up to 40ms.

LED Constant-Current Setting Register (0x43)

The LED constant-current setting register sets the global constant-current level (see Table 18 in the *Register Tables* section). Bit D0 selects the global current values between 10mA and 20mA. This setting only applies to the LED driver enabled pins, PORT15–PORT12.

Common PWM Ratio Register (0x45)

The common PWM ratio register stores the common constant-current output PWM duty cycle (see Table 19 in the *Register Tables* section). The values stored in this register translate over to a PWM ratio in the same manner as the individual PWM ratio registers (0x50 to 0x53). Ports can use their own individual PWM value or the common PWM value. Write to this register to change the PWM ratio of several ports at once.

I²C Timeout Flag Register (0x48) (Read Only)

The I²C timeout flag register contains a single bit (D0), which indicates if an I²C timeout has occurred (see Table 20 in the *Register Tables* section). Read this register to clear an I²C timeout initiated interrupt.

PORT12–PORT15 Individual PWM Ratio Registers (0x50 to 0x53)

Each LED driver port has an individual PWM ratio register, 0x50 to 0x53 (see Table 21 in the *Register Tables* section). Use values 0x00 to 0xFE in these registers to configure the number of cycles out of 256 the output sinks current (LED is on), from 0 cycles to 254 cycles. Use 0xFF to have an output continuously sink current (always on). For applications requiring multiple ports to have the same intensity, program a particular port's configuration register (0x54 to 0x57) to use the common PWM ratio register (0x45). New PWM settings take place at the beginning of a PWM cycle, to allow changes from common intensity to individual intensity with no interruption in the PWM cycle.

PORT12–PORT15 LED Configuration Registers (0x54 to 0x57)

Registers 0x54 to 0x57 set individual configurations for each port (see Table 22 in the *Register Tables* section). D5 sets the port's PWM setting to either the common or individual PWM setting. Bits D[4:2] enable and set the port's individual blink period from 0 to 4096ms. Bits D1 and D0 set a port's blink duty cycle.

Interrupt Mask 1 and 2 Registers (0x58, 0x59)

The interrupt mask 1 and 2 registers control which ports trigger an interrupt for PORT7–PORT0 and PORT15–PORT8, respectively (see Tables 23 and 24 in the *Register Tables* section). Set the bit to 0 to enable the interrupt. Set the bit to 1 to mask the interrupt.

If the port that has generated the interrupt is not masked, the interrupt causes the $\overline{INT}$ signal to assert. A read of the GPIO values 1 and 2 registers (0x3A, 0x3B) is required to deassert the $\overline{INT}$ pin. Note that transitions that occur while the $\overline{INT}$ signal is asserted, but before the read of

the values 1 and 2 registers, sets the appropriate bit of the values 1 and 2 registers only, but has no effect on the $\overline{INT}$ pin as it is already asserted. However, transitions that occur when the I²C is active cannot be latched into the values 1 and 2 registers until after the read has taken place. If there are transitions that cause the $\overline{INT}$ signal to assert, during the time of an I²C read, they cause the $\overline{INT}$ signal to reassert once the read transaction has taken place. Note that the interrupt configurations only apply when a port is configured as an input.

GPI Trigger Mode 1 and 2 Registers (0x5A, 0x5B)

The GPI trigger mode 1 and 2 registers control how ports can trigger an interrupt for PORT7–PORT0 and PORT15–PORT8, respectively (see Tables 25 and 26 in the *Register Tables* section). Set the bit to 0 for rising-edge triggering. Set the bit to 1 for rising- and falling-edge triggering.

The inputs are debounced (if enabled) by taking a snapshot of the port state when the transition occurs, and another after the debounce time has elapsed—ensuring that the state of the port is stable prior to triggering the interrupt. After the debounce cycle, an interrupt is generated and the $\overline{INT}$ pin asserts if it is not masked for that particular port. Regardless of whether or not the $\overline{INT}$ signal is masked, the GPIO values 1 and 2 registers (0x3A, 0x3B) report the state of all input ports.

Sleep Mode

The device is put into sleep mode by clearing bit D4 in the GPIO global configuration register (0x40). In sleep mode, the device draws minimal current. The device is taken out of sleep mode and put into operating mode by setting bit D4 in the GPIO configuration register. When the GPIOs are enabled, the part is in operating mode.

In sleep mode, the internal oscillator and I²C timeout features are disabled.

LED Fade

Set the fade cycle time in the GPIO global configuration register (0x40) to a non-zero value to enable fade in/out (see Table 16 in the *Register Tables* section). Fade in increases an LED's PWM intensity in 16 even steps, from zero to its stored value. Fade out decreases an LED's PWM intensity in 16 even steps, from its current value to zero. Fading occurs automatically in any of the following scenarios:

1) Change the common PWM register value from any value to zero to cause all ports using the common PWM register settings to fade out. No ports using individual PWM settings are affected.
2) Change the common PWM register value to any value from zero to cause all ports using the common PWM register settings to fade in. No ports using individual PWM settings are affected.
3) Take the part out of sleep mode to cause all ports to fade in. Changing an individual PWM intensity during fade in automatically cancels that port's fade and immediately outputs at its newly programmed intensity.
4) Put the part into sleep mode to cause all ports to fade out. Changing an individual PWM intensity during fade out automatically cancels that port's fade and immediately turns off.

LED PWM

Each port has an individual PWM ratio register. The value stored in this register configures the number of cycles out of 255 that the output is sinking current (LED is on). Setting a value of 0xFF in an individual intensity register sets the output to continuously sink current (always on). Conversely, setting a value of 0x00 in an individual intensity register sets the output in a high-impedance state (always off).

For applications requiring multiple ports to have the same intensity, the common PWM ratio intensity setting can be used in lieu of the individual intensity setting. To use the common intensity setting, program bit D5 of the corresponding port's configuration register to logic-high. Setting a port to use the common PWM ratio setting copies the value of the common intensity register into the individual intensity register at the beginning of each PWM cycle. This allows an output port to be seamlessly changed from common intensity to individual intensity with no interruption in the PWM cycle.

Outputs are configured to sink a constant current of either 10mA or 20mA during the period when the output is on. The setting in the individual constant-current setting register (0x43) controls the value of the current.

LED Blink

Each LED driver-supported port has its own blink-control settings through registers 0x54 to 0x57 (see Table 22 in the *Register Tables* section). The blink period ranges from 0 (blink disabled) to 4.096s. Settable blink duty cycles range from 6.25% to 50%. All blink periods start at the same PWM cycle for synchronized blinking between multiple ports.

Each port has its own counter to generate blink timing. The blink counter can be programmed to cause the output to gate off and on at a programmable rate. The blink period can be set to 256ms, 512ms, 1.024s, 2.048s, or 4.096s using D[4:2] of the port's individual configuration register. The percentage of time that the LED is on for one blink cycle is set to 50%, 25%, 12.5%, or 6.25% by D[1:0] of the individual configuration register.

Interrupt

Two possible sources generate $\overline{INT}$: I2C timeout or GPIOs configured as inputs (registers 0x48, 0x5A, and 0x5B). Read the respective data/status registers for each type of interrupt in order to clear $\overline{INT}$. If multiple sources generate the interrupt, all the related status registers must be read to clear $\overline{INT}$.

Serial Interface

Figure 1 shows the 2-wire serial interface timing details.

Serial Addressing

The device operates as a slave that sends and receives data through an I2C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer.

The device's SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The device's SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START (S) condition (Figure 2) sent by a master, followed by the device's 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally, a STOP (P) condition.

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

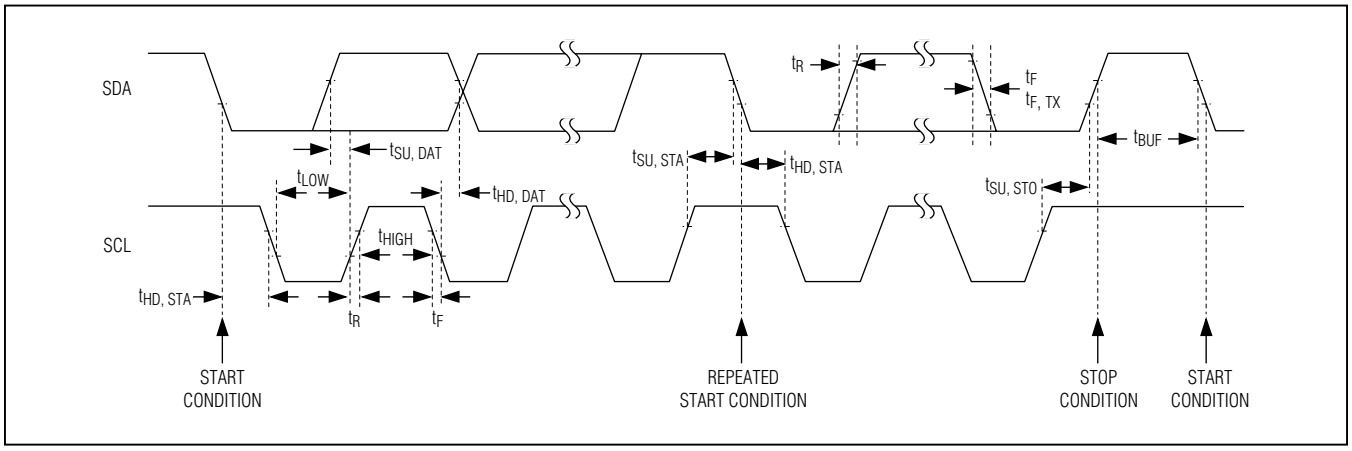


Figure 1. Two-Wire Serial Interface Timing Details

Bit Transfer

One data bit is transferred during each clock pulse (Figure 3). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 4), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits.

The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse; therefore, the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the device, the device generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

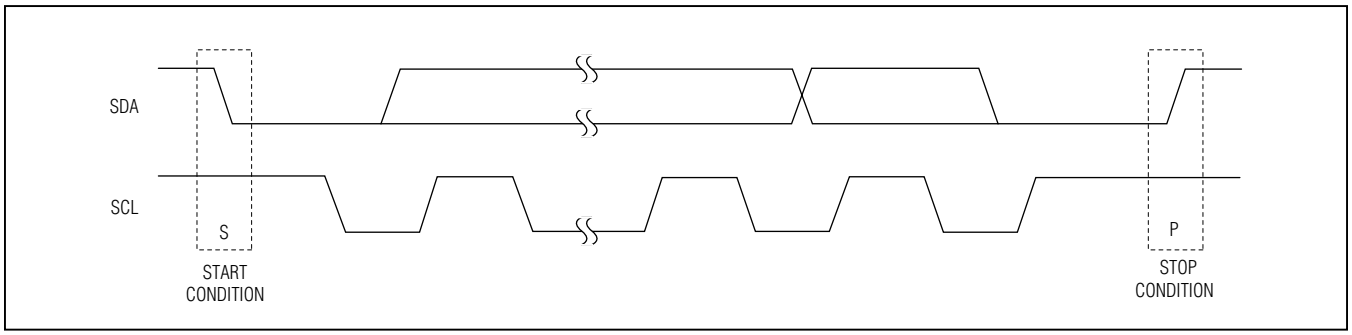


Figure 2. START and STOP Conditions

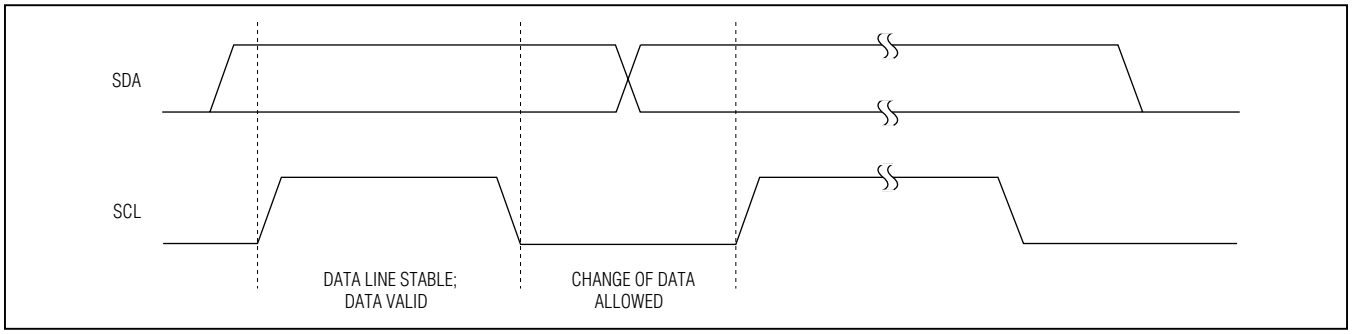


Figure 3. Bit Transfer

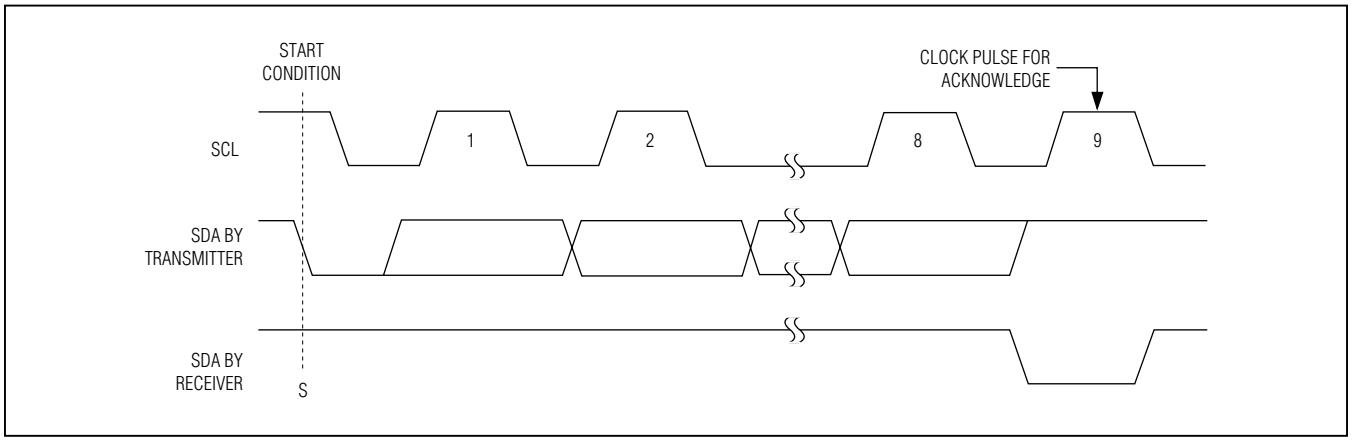


Figure 4. Acknowledge

Slave Addresses

The device has two 7-bit long slave addresses. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

The first 4 bits (MSBs) of the device slave addresses are always 0111. Slave address bits A[3:1] correspond, by the matrix in Table 2, to the states of the device address input pin AD0, and A0 corresponds to the R/$\overline{W}$ bit (Figure 5). The AD0 input can be connected to any of four signals: GND, V_{CC}, SDA, or SCL, giving four possible slave-address pairs, allowing up to four devices to share the same bus. Because SDA and SCL are dynamic signals, care must be taken to ensure that AD0 transitions no sooner than the signals on SDA and SCL.

The device monitors the bus continuously, waiting for a START condition followed by its slave address. When the device recognizes its slave address, it acknowledges and is then ready for continued communication.

Table 2. 2-Wire Interface Address Map

PIN AD0	DEVICE ADDRESS							
	A7	A6	A5	A4	A3	A2	A1	A0
GND	0	1	1	1	0	0	0	R/$\overline{W}$
V_{CC}					0	1		
SDA					1	0		
SCL					1	1		

Bus Timeout

The device features a 20ms (min) bus timeout on the 2-wire serial interface, largely to prevent the device from holding the SDA I/O low during a read transaction, should the SCL lock up for any reason before a serial transaction is completed. Bus timeout operates by causing the device to internally terminate a serial transaction, either read or write, if the time between adjacent edges on SCL exceeds 20ms. After a bus timeout, the device waits for a valid START condition before responding to a consecutive transmission. This feature can be enabled or disabled under user control by writing to the configuration register.

Message Format for Writing

A write to the device comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least one byte of information. The first byte of information is the command byte. The command byte determines which register of the device is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, the device takes no further action (Figure 6) beyond storing the command byte.

Any bytes received after the command byte are data bytes. The first data byte goes into the internal register of the device selected by the command byte (Figure 7).

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent device internal registers, because the command byte address generally autoincrements.

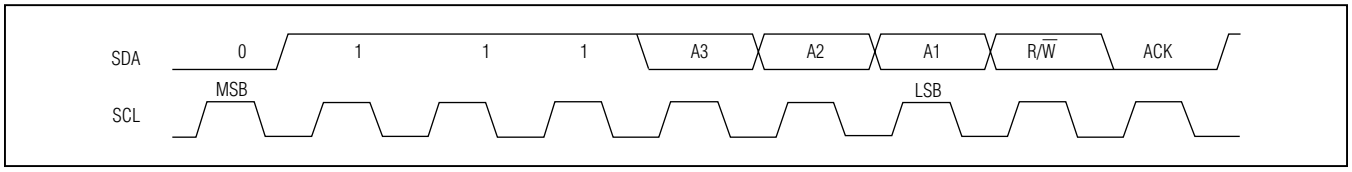


Figure 5. Slave Address

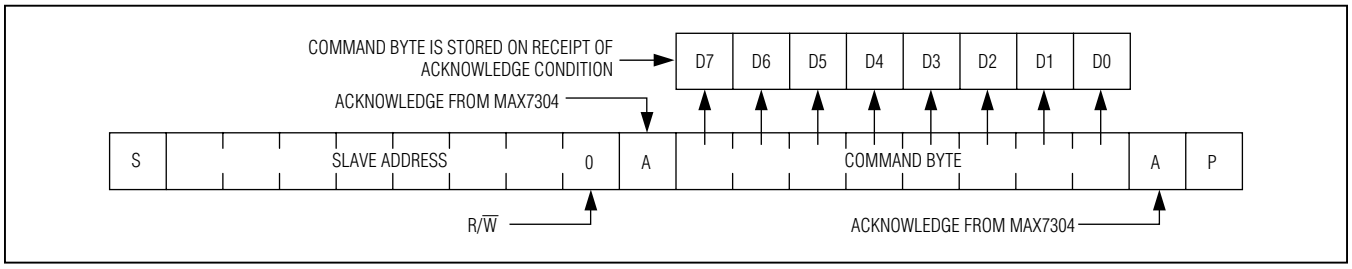


Figure 6. Command Byte Received

Message Format for Reading

The device is read using the internally stored command byte as an address pointer, the same way the stored command byte is used as an address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the device's command byte by performing a write (Figure 6). The master can now read N consecutive bytes from the device, with the first data byte being read from the register addressed by the initialized command byte. When performing read-after-write verification, remember to reset the command byte's address because the stored command byte address is generally autoincremented after the write (Figure 8).

Operation with Multiple Masters

When the device is operated on a 2-wire interface with multiple masters, a master reading the device uses a repeated START between the write that sets the device's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the device's address pointer but before master 1 has read the data. If master 2 subsequently resets the device's address pointer, master 1's read can be from an unexpected location.

Command Address Autoincrementing

Address autoincrementing allows the device to be configured with fewer transmissions by minimizing the number of times the command address needs to be sent. The command address (0x31 to 0x5B) stored in the device increments after each data byte is written or read. Autoincrement only functions when doing a multiburst read or write.

Applications Information

Reset from I²C

After a catastrophic event such as ESD discharge or microcontroller reset, use bit D4 of the GPIO global configuration register (0x40) as a software reset.

Hot Insertion

The $\overline{INT}$, SCL, and AD0 inputs and SDA remain high impedance with up to 5.5V asserted on them when the device powers down (V_{CC} = 0V). I/O ports remain high impedance with up to 5.5V asserted on them when not powered. Use the device in hot-swap applications.

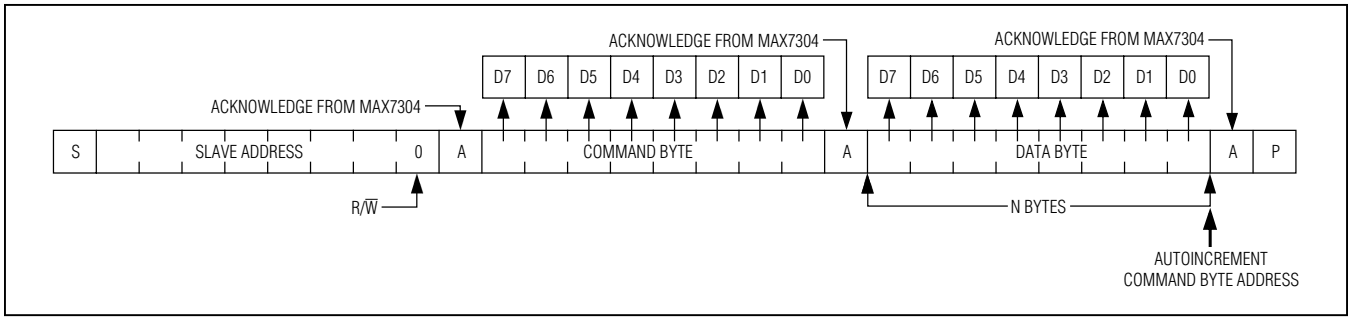


Figure 7. Command and Single Data Byte Received

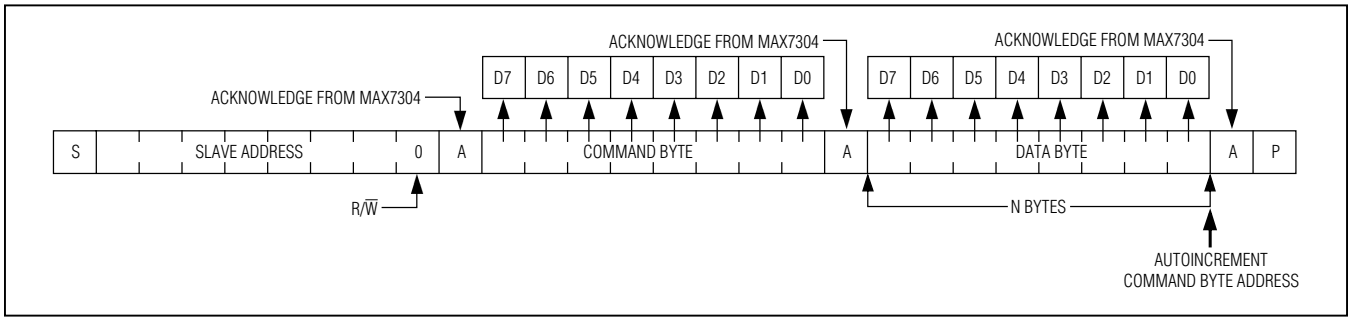


Figure 8. N Data Bytes Received

Staggered PWM

The LED's on-time in each PWM cycle is phase delayed by 45° into four evenly spaced start positions. Optimize phasing when using fewer than four ports as constant-current outputs by allocating the ports with the most appropriate start positions. For example, if using two constant-current outputs, choose PORT12 and PORT14 because their PWM start positions are evenly spaced. In general, choose the ports that spread the current demand from the ports' load supply.

Power-Supply Considerations

The device operates with a 1.62V to 3.6V power-supply voltage. Bypass the power supply V_{CC} to GND with a 0.1µF or higher ceramic capacitor as close as possible to the device. Bypass the logic power supply (V_{LA}) to GND with a 0.1µF or higher ceramic capacitor as close as possible to the device.

ESD Protection

All device pins meet the ±2.5kV Human Body Model ESD tolerances. The GPIOs meet IEC 61000-4-2 ESD protection. The IEC test stresses consist of 10 consecutive ESD discharges per polarity at the maximum specified level and below (per IEC 61000-4-2). Test criteria include:

1) The powered device does not latch up during the ESD discharge event.
2) The device subsequently passes the final test used for prescreening.

Tables 3 and 4 are from the IEC 61000-4-2: Edition 1.1 1999-05: *Electromagnetic compatibility (EMC) Testing and measurement techniques—Electrostatic discharge immunity test*.

Table 3. ESD Test Levels

1A—CONTACT DISCHARGE		1B—AIR DISCHARGE	
LEVEL	**TEST VOLTAGE (kV)**	**LEVEL**	**TEST VOLTAGE (kV)**
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
X	Special	X	Special

X = Open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment could be needed.

Table 4. ESD Waveform Parameters

LEVEL	INDICATED VOLTAGE (kV)	FIRST PEAK OF CURRENT DISCHARGE ±10% (A)	RISE TIME (t_R) WITH DISCHARGE SWITCH (ns)	CURRENT (±30%) AT 30ns (A)	CURRENT (±30%) AT 60ns (A)
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

Table 5. Configuration Register (0x01)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:1]	Reserved	—	—	0000101
D0	Timeout disable	0	I²C timeout enabled	1
		1	I²C timeout disabled	

Table 6. LED Driver Enable Register (0x31)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:4]	Reserved	0000	—	0000
D3	PORT15	0	GPIO function	0
		1	LED driver enable	
D2	PORT14	0	GPIO function	0
		1	LED driver enable	
D1	PORT13	0	GPIO function	0
		1	LED driver enable	
D0	PORT12	0	GPIO function	0
		1	LED driver enable	

Table 7. GPIO Direction 1 Register (0x34)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT7	0	Set as input pin	0
		1	Set as output pin	
D6	PORT6	0	Set as input pin	0
		1	Set as output pin	
D5	PORT5	0	Set as input pin	0
		1	Set as output pin	
D4	PORT4	0	Set as input pin	0
		1	Set as output pin	
D3	PORT3	0	Set as input pin	0
		1	Set as output pin	
D2	PORT2	0	Set as input pin	0
		1	Set as output pin	
D1	PORT1	0	Set as input pin	0
		1	Set as output pin	
D0	PORT0	0	Set as input pin	0
		1	Set as output pin	

Table 8. GPIO Direction 2 Register (0x35)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT15	0	Set as input pin	0
		1	Set as output pin	
D6	PORT14	0	Set as input pin	0
		1	Set as output pin	
D5	PORT13	0	Set as input pin	0
		1	Set as output pin	
D4	PORT12	0	Set as input pin	0
		1	Set as output pin	
D3	PORT11	0	Set as input pin	0
		1	Set as output pin	
D2	PORT10	0	Set as input pin	0
		1	Set as output pin	
D1	PORT9	0	Set as input pin	0
		1	Set as output pin	
D0	PORT8	0	Set as input pin	0
		1	Set as output pin	

Table 9. GPO Output Mode 1 Register (0x36)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT7	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D6	PORT6	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D5	PORT5	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D4	PORT4	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D3	PORT3	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D2	PORT2	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D1	PORT1	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D0	PORT0	0	Port is an open-drain output	1
		1	Port is a push-pull output	

Table 10. GPO Output Mode 2 Register (0x37)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT15	0	Port is an open-drain output	0
D6	PORT14	0	Port is an open-drain output	0
D5	PORT13	0	Port is an open-drain output	0
D4	PORT12	0	Port is an open-drain output	0
D3	PORT11	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D2	PORT10	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D1	PORT9	0	Port is an open-drain output	1
		1	Port is a push-pull output	
D0	PORT8	0	Port is an open-drain output	1
		1	Port is a push-pull output	

Note: *When programmed as GPO, PORT15–PORT12 are always open-drain and bits D[7:4] are not writable.*

Table 11. GPIO Supply Voltage 1 Register (0x38)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT7	0	PORT7 supplied by V_{CC}	0
		1	PORT7 supplied by V_{LA}	
D6	PORT6	0	PORT6 supplied by V_{CC}	0
		1	PORT6 supplied by V_{LA}	
D5	PORT5	0	PORT5 supplied by V_{CC}	0
		1	PORT5 supplied by V_{LA}	
D4	PORT4	0	PORT4 supplied by V_{CC}	0
		1	PORT4 supplied by V_{LA}	
D3	PORT3	0	PORT3 supplied by V_{CC}	0
		1	PORT3 supplied by V_{LA}	
D2	PORT2	0	PORT2 supplied by V_{CC}	0
		1	PORT2 supplied by V_{LA}	
D1	PORT1	0	PORT1 supplied by V_{CC}	0
		1	PORT1 supplied by V_{LA}	
D0	PORT0	0	PORT0 supplied by V_{CC}	0
		1	PORT0 supplied by V_{LA}	

Table 12. GPIO Supply Voltage 2 Register (0x39)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT15	0	PORT15 supplied by V_{CC}	0
		1	PORT15 supplied by V_{LA}	
D6	PORT14	0	PORT14 supplied by V_{CC}	0
		1	PORT14 supplied by V_{LA}	
D5	PORT13	0	PORT13 supplied by V_{CC}	0
		1	PORT13 supplied by V_{LA}	
D4	PORT12	0	PORT12 supplied by V_{CC}	0
		1	PORT12 supplied by V_{LA}	
D3	PORT11	0	PORT11 supplied by V_{CC}	0
		1	PORT11 supplied by V_{LA}	
D2	PORT10	0	PORT10 supplied by V_{CC}	0
		1	PORT10 supplied by V_{LA}	
D1	PORT9	0	PORT9 supplied by V_{CC}	0
		1	PORT9 supplied by V_{LA}	
D0	PORT8	0	PORT8 supplied by V_{CC}	0
		1	PORT8 supplied by V_{LA}	

Table 13. GPIO Values 1 Register (0x3A)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT7	0	Clear PORT7 low	1
		1	Set PORT7 high	
D6	PORT6	0	Clear PORT6 low	1
		1	Set PORT6 high	
D5	PORT5	0	Clear PORT5 low	1
		1	Set PORT5 high	
D4	PORT4	0	Clear PORT4 low	1
		1	Set PORT4 high	
D3	PORT3	0	Clear PORT3 low	1
		1	Set PORT3 high	
D2	PORT2	0	Clear PORT2 low	1
		1	Set PORT2 high	
D1	PORT1	0	Clear PORT1 low	1
		1	Set PORT1 high	
D0	PORT0	0	Clear PORT0 low	1
		1	Set PORT0 high	

Table 14. GPIO Values 2 Register (0x3B)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT15	0	Clear PORT15 low	1
		1	Set PORT15 high*	
D6	PORT14	0	Clear PORT14 low	1
		1	Set PORT14 high*	
D5	PORT13	0	Clear PORT13 low	1
		1	Set PORT13 high*	
D4	PORT12	0	Clear PORT12 low	1
		1	Set PORT12 high*	
D3	PORT11	0	Clear PORT11 low	1
		1	Set PORT11 high	
D2	PORT10	0	Clear PORT10 low	1
		1	Set PORT10 high	
D1	PORT9	0	Clear PORT9 low	1
		1	Set PORT9 high	
D0	PORT8	0	Clear PORT8 low	1
		1	Set PORT8 high	

**Open-drain output, pullup resistor required.*

Table 15. GPIO Level-Shifter Enable (0x3C)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT7/PORT15	0	Level shifting disabled	0
		1	Level shift between PORT7 and PORT15 enabled; direction controlled by GPIO direction 2 register (0x35)	
D6	PORT6/PORT14	0	Level shifting disabled	0
		1	Level shift between PORT6 and PORT14 enabled; direction controlled by GPIO direction 2 register (0x35)	
D5	PORT5/PORT13	0	Level shifting disabled	0
		1	Level shift between PORT5 and PORT13 enabled; direction controlled by GPIO direction 2 register (0x35)	
D4	PORT4/PORT12	0	Level shifting disabled	0
		1	Level shift between PORT4 and PORT12 enabled; direction controlled by GPIO direction 2 register (0x35)	
D3	PORT3/PORT11	0	Level shifting disabled	0
		1	Level shift between PORT3 and PORT11 enabled; direction controlled by GPIO direction 2 register (0x35)	
D2	PORT2/PORT10	0	Level shifting disabled	0
		1	Level shift between PORT2 and PORT10 enabled; direction controlled by GPIO direction 2 register (0x35)	

Table 15. GPIO Level-Shifter Enable (0x3C) (continued)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D1	PORT1/PORT9	0	Level shifting disabled	0
		1	Level shift between PORT1 and PORT9 enabled; direction controlled by GPIO direction 2 register (0x35)	
D0	PORT0/PORT8	0	Level shifting disabled	0
		1	Level shift between PORT0 and PORT8 enabled; direction controlled by GPIO direction 2 register (0x35)	

Table 16. GPIO Global Configuration Register (0x40)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:6]	Reserved	0	—	00
D5	I2C timeout interrupt enable	0	Disabled	0
		1	$\overline{INT}$ is asserted when I2C bus times out. $\overline{INT}$ is deasserted when a read is performed on the I2C timeout flag register (0x48).	
D4	GPIO enable	0	PWM, constant-current circuits, and GPIs are shut down. GPO values depend on their setting. Register 0x31 to 0x5B values are stored and cannot be changed. The entire part is shut down.	0
		1	Normal GPIO operation. PWM, constant-current circuits, and GPIOs are enabled.	
D3	GPIO reset	0	Normal operation.	0
		1	Return all GPIO registers (registers 0x31 to 0x5B) to their POR value. This bit is momentary and resets itself to 0 after the write cycle.	
D[2:0]	Fade-in/out time	000	No fading.	000
		XXX	PWM intensity ramps up (down) between the common PWM value and 0% duty cycle in 16 steps over the following time period: D[2:0] = 001 = 256ms D[2:0] = 010 = 512ms D[2:0] = 011 = 1024ms D[2:0] = 100 = 2048ms D[2:0] = 101 = 4096ms D[2:0] = 110/111 = Undefined	

Table 17. GPIO Debounce Configuration Register (0x42)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	RESERVED			DEBOUNCE TIME				
Power-up default setting Debounce time is 9ms	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Debounce time is 10ms	0	0	0	0	0	0	0	1
Debounce time is 11ms	0	0	0	0	0	0	1	0
Debounce time is 12ms	0	0	0	0	0	0	1	1
⋮								
Debounce time is 37ms	0	0	0	1	1	1	0	0
Debounce time is 38ms	0	0	0	1	1	1	0	1
Debounce time is 39ms	0	0	0	1	1	1	1	0
Debounce time is 40ms	0	0	0	1	1	1	1	1

Table 18. LED Constant-Current Setting Register (0x43)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:6]	Reserved	11	Set always as 11	11
D[5:1]	Reserved	00000	—	00000
D0	Constant-current setting	0	Constant current is 20mA	0
		1	Constant current is 10mA	

Table 19. Common PWM Ratio Register (0x45)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	COMMON PWM							
Power-up default setting Common PWM ratio is 0/256	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Common PWM ratio is 1/256	0	0	0	0	0	0	0	1
Common PWM ratio is 2/256	0	0	0	0	0	0	1	0
Common PWM ratio is 3/256	0	0	0	0	0	0	1	1
⋮								
Common PWM ratio is 252/256	1	1	1	1	1	1	0	0
Common PWM ratio is 253/256	1	1	1	1	1	1	0	1
Common PWM ratio is 254/256	1	1	1	1	1	1	1	0
Common PWM ratio is **256/256** (100% duty cycle)	1	1	1	1	1	1	1	1

Table 20. I²C Timeout Flag Register (0x48) (Read Only)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:1]	Reserved	0000000	—	0000000
D0	I²C timeout flag	0	No I²C timeout has occurred since last read or POR.	0
		1	I²C timeout has occurred since last read or POR. This bit is reset to zero when a read is performed on this register. I²C timeouts must be enabled for this function to work (see Table 5).	

Table 21. PORT12–PORT15 Individual PWM Ratio Registers (0x50 to 0x53)

REGISTER DESCRIPTION	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
	PORT PWM							
Power-up default setting PORT PWM ratio is 0/256	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
PORT PWM ratio is 1/256	0	0	0	0	0	0	0	1
PORT PWM ratio is 2/256	0	0	0	0	0	0	1	0
PORT PWM ratio is 3/256	0	0	0	0	0	0	1	1
⋮								
PORT PWM ratio is 252/256	1	1	1	1	1	1	0	0
PORT PWM ratio is 253/256	1	1	1	1	1	1	0	1
PORT PWM ratio is 254/256	1	1	1	1	1	1	1	0
PORT PWM ratio is **256/256** (100% duty cycle)	1	1	1	1	1	1	1	1

Table 22. PORT12–PORT15 LED Configuration Registers (0x54 to 0x57)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D[7:6]	Don't care	00	—	00
D5	Common PWM	0	Port uses individual PWM intensity register to set the PWM ratio	0
		1	Port uses common PWM intensity register to set the PWM ratio	
D[4:2]	Blink period	000	Port does not blink	000
		001	Port blink period is 256ms	
		010	Port blink period is 512ms	
		011	Port blink period is 1024ms	
		100	Port blink period is 2048ms	
		101	Port blink period is 4096ms	
		110/111	Undefined	
D[1:0]	Blink-on time	00	LED is on for 50% of the blink period	00
		01	LED is on for 25% of the blink period	
		10	LED is on for 12.5% of the blink period	
		11	LED is on for 6.25% of the blink period	

Table 23. Interrupt Mask 1 Register (0x58)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT7	0	Interrupt is not masked	1
		1	Interrupt is masked	
D6	PORT6	0	Interrupt is not masked	1
		1	Interrupt is masked	
D5	PORT5	0	Interrupt is not masked	1
		1	Interrupt is masked	
D4	PORT4	0	Interrupt is not masked	1
		1	Interrupt is masked	
D3	PORT3	0	Interrupt is not masked	1
		1	Interrupt is masked	
D2	PORT2	0	Interrupt is not masked	1
		1	Interrupt is masked	
D1	PORT1	0	Interrupt is not masked	1
		1	Interrupt is masked	
D0	PORT0	0	Interrupt is not masked	1
		1	Interrupt is masked	

Table 24. Interrupt Mask 2 Register (0x59)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT15	0	Interrupt is not masked	1
		1	Interrupt is masked	
D6	PORT14	0	Interrupt is not masked	1
		1	Interrupt is masked	
D5	PORT13	0	Interrupt is not masked	1
		1	Interrupt is masked	
D4	PORT12	0	Interrupt is not masked	1
		1	Interrupt is masked	
D3	PORT11	0	Interrupt is not masked	1
		1	Interrupt is masked	
D2	PORT10	0	Interrupt is not masked	1
		1	Interrupt is masked	
D1	PORT9	0	Interrupt is not masked	1
		1	Interrupt is masked	
D0	PORT8	0	Interrupt is not masked	1
		1	Interrupt is masked	

Table 25. GPI Trigger Mode 1 Register (0x5A)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT15	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D6	PORT14	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D5	PORT13	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D4	PORT12	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D3	PORT11	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D2	PORT10	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D1	PORT9	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D0	PORT8	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	

Table 26. GPI Trigger Mode 2 Register (0x5B)

REGISTER BIT	DESCRIPTION	VALUE	FUNCTION	DEFAULT VALUE
D7	PORT15	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D6	PORT14	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D5	PORT13	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D4	PORT12	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D3	PORT11	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D2	PORT10	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D1	PORT9	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	
D0	PORT8	0	Rising-edge-triggered interrupts	0
		1	Rising- and falling-edge-triggered interrupts	

Wafer-Level Packaging (WLP) Applications Information

For the latest application details on WLP construction, dimensions, tape-carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*, available at www.maximintegrated.com.

Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX7304ETG+	-40°C to +85°C	24 TQFN-EP*
MAX7304EWA+**	-40°C to +85°C	25 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN-EP	T243A3+1	21-0188	90-0122
25 WLP	W252F2+1	21-0453	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	3/12	Updated ESD protection specifications	1, 4, 8, 16
2	5/15	Updated Table 1	8