PIC18F87J10 Family Rev. A3 Silicon Errata

The PIC18F87J10 family parts you have received conform functionally to the Device Data Sheet (DS39663**D**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F87J10 family will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F87J10 family devices with these Device/ Revision IDs:

Part Number	Device ID	Revision ID
PIC18F65J10	0001 0101 001	0 0100
PIC18F65J15	0001 0101 010	0 0100
PIC18F66J10	0001 0101 011	0 0100
PIC18F66J15	0001 0101 100	0 0100
PIC18F67J10	0001 0101 101	0 0100
PIC18F85J10	0001 0101 111	0 0100
PIC18F85J15	0001 0111 000	0 0100
PIC18F86J10	0001 0111 001	0 0100
PIC18F86J15	0001 0111 010	0 0100
PIC18F87J10	0001 0111 011	0 0100

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: Flash Program Memory

Writes to program memory address 300000h, that are not blocked, can cause the program memory at different locations to be corrupted.

Work around

Do not write to address 300000h. If you wish to modify the contents of the Configuration registers, then modify the Configuration Words located at the end of the user memory and issue a Reset command. This will reload the Configuration registers with the new configuration setting.

The end of the user memory is:

- PIC18FX5J10 devices — 7FF4h
- PIC18FX5J10 devices — 3FF4h

For additional information, see the Device Data Sheet (DS39663), **Section 23.1 "Configuration Bits"**.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: External Memory Bus

For PIC18F8XJXX devices, the Stack Pointer may incorrectly increment during a table read operation if the external memory bus wait states are enabled.

This is when:

- The Configuration bit, WAIT, is clear (CONFIG3L<7> = 0)
- The WAITx bits (MEMCON<5:4>) are *not* equal to '11'

Work around

If using the external memory bus and performing TBLRD operations with a non-zero wait state – described by the preceding two bullet points – first disable interrupts by clearing the GIE/GIEH (INTCON<7>) and PEIE/GIEL (INTCON<6>) bits.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: External Memory Bus

The A<19:16> EMB address lines and read/write control pins ($\overline{OE}$, $\overline{WRH}$ and $\overline{WRL}$) are released to their respective inactive states at the same time which violates the timing condition mentioned in Figure 26-5 and Figure 26-6 in the data sheet.

This may result in the peripheral device on the bus detecting an address change when write/read is initiated. The bus capacitance and signal delay on the address and control lines can affect the probability of invalid detection.

Work around

Do one of the following:

- Use a latch based on the falling edge of ALE to hold the A<19:16> signals.
- Add a delay circuit to extend the valid time for A<19:16> signals to ensure the address is valid until read/write signals go inactive.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Timer1

In 16-Bit Asynchronous Counter mode (with or without use of the Timer1 oscillator), the TMR1H and TMR3H buffers do not update when TMRxL is read.

This issue only affects reading the TMRxH registers. The timers increment and set the interrupt flags as expected and the Timer registers can be written as expected.

Work around

1. Use 8-bit mode by clearing the RD16 bit (T1CON<7>).
2. Use the internal clock synchronization option by clearing the $\overline{\text{T1SYNC}}$ bit (T1CON<2>).

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: Master Synchronous Serial Port (MSSP)

In SPI mode, the following bits are not reset upon disabling the SPI module (by clearing the SSPEN bit in SSPxCON1 register):

- Buffer Full bit – BF in SSPxSTAT register
- Write Collision Detect bit – WCOL in SSPxCON1
- Receive Overflow Indicator bit – SSPOV in SSPxCON1

For example, if SSPxBUF is full (BF bit is set) and the MSSP module is disabled and re-enabled, the BF bit will remain set. In SPI Slave mode, that can mean:

- A subsequent write to SSPxBUF will result in a write collision
- A new byte will cause a receive overflow

Work around

Before disabling the MSSP module, ensure that:

- WCOL is clear
- If the buffer is full, SSPxBUF is read (thus clearing the BF flag)
- If the module was configured in SPI Slave mode, the SSPOV bit is clear

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: Master Synchronous Serial Port (MSSP)

In its current implementation, the Baud Rate Generator for I^2C™ in Master mode is slower than the rates specified in Table 17-3 of the Device Data Sheet.

For this revision of silicon:

- For the I^2C clock rates – use the values shown in Table 1 in place of those shown in Table 18-3 of the Device Data Sheet. (The differences are shown in **bold** text.)
- For bit description, SSPM3:SSPM0 = `1000`, use the following formula in place of the one shown in Register 18-2 (SSPxCON1) of the Device Data Sheet.

$$SSPADD = INT((F_{CY}/F_{SCL}) - (F_{CY}/1.111\ MHz)) - 1$$

Note: The I^2C bus is a synchronous protocol, so the accuracy of the bus frequency is not critical.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: I^2C™ CLOCK RATE with BRG

FOSC	FCY	FCY * 2	BRG Value	FSCL (2 Rollovers of BRG)
40 MHz	10 MHz	20 MHz	**0Eh**	400 kHz(1)
40 MHz	10 MHz	20 MHz	**15h**	312.5 kHz
40 MHz	10 MHz	20 MHz	**59h**	100 kHz
16 MHz	4 MHz	8 MHz	**05h**	400 kHz(1)
16 MHz	4 MHz	8 MHz	**08h**	308 kHz
16 MHz	4 MHz	8 MHz	**23h**	100 kHz
4 MHz	1 MHz	2 MHz	**01h**	333 kHz(1)
4 MHz	1 MHz	2 MHz	**08h**	100 kHz
4 MHz	1 MHz	2 MHz	00h	1 MHz(1)

Note 1: The I^2C™ interface does not conform to the 400 kHz I^2C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

7. Module: Master Synchronous Serial Port (MSSP)

After an I^2C transfer is initiated, the SSPxBUF register may be written for up to 10 TCY before additional writes are blocked. The data transfer may be corrupted if SSPxBUF is written during this time.

The WCOL bit is set any time an SSPxBUF write occurs during a transfer.

Work around

Avoid writing SSPxBUF until the data transfer is complete, indicated by the setting of the SSP1IF bit (PIR1<3>).

Verify the WCOL bit (SSPxCON1<7>) is clear after writing SSPxBUF to ensure any potential transfer in progress is not corrupted.

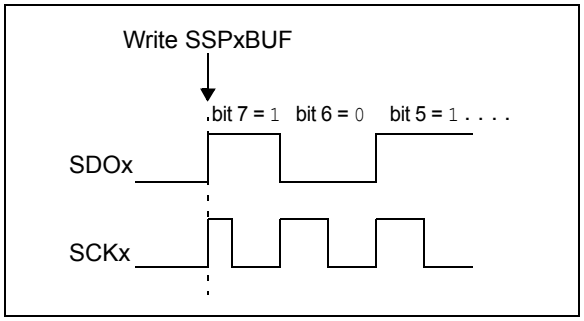
Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: Master Synchronous Serial Port (MSSP)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCKx pulse may occur on the first bit of the transmitted/received data. See Figure 1.

FIGURE 1: SCKx PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse:

1. Turn off Timer2.
2. Clear the TMR2 register.
3. Load the SSPxBUF with the data to be transmitted.
4. Turn Timer2 back on.

For sample code, see Example 1.

EXAMPLE 1: AVOIDING THE INITIAL SHORT SCK1 PULSE (FOR MSSP1)

```
LOOP BTFSS  SSP1STAT, BF    ;Data received?
                            ;(Xmit complete?)
     BRA    LOOP            ;No
     MOVF   SSP1BUF, W      ;W = SSPBUF
     MOVWF  RXDATA          ;Save in user RAM
     MOVF   TXDATA, W       ;W = TXDATA
     BCF    T2CON, TMR2ON   ;Timer2 off
     CLRF   TMR2            ;Clear Timer2
     MOVWF  SSP1BUF         ;Xmit New data
     BSF    T2CON, TMR2ON   ;Timer2 on
```

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: Master Synchronous Serial Port (MSSP)

In SPI mode, the SDOx output may change after the inactive clock edge of the bit '0' output. This may affect some SPI components that read data more than 300 ns after the inactive edge of SCKx.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: Master Synchronous Serial Port (MSSP)

When the MSSP peripherals are configured for SPI mode, the Buffer Full bit, BF (SSPxSTAT<0>) should *not* be polled in software to determine when the transfer is complete.

Work around

Do one of the following:

- Copy the SSPxSTAT register into a variable and perform the bit test on the variable. (Example 2 copies SSP1STAT into the working register where the bit test is performed.)

EXAMPLE 2: Master Synchronous Serial Port (MSSP1)

```
loop_MSB:
    MOVF   SSP1STAT, W
    BTFSS  WREG, BF
    BRA    loop_MSB
```

- Poll the Master Synchronous Serial Port Interrupt Flag bit, SSP1IF (PIR1<3>). This bit can be polled and will set when the transfer is complete.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted; only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the transmit buffer, TXREGx, are transferred to the TSR during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- The TXREGx is written to
- The baud rate counter overflows (at the end of the bit period)
- A Stop bit is transmitted (shifted out of TSR)

Work around

If possible, do not use the module's double-buffer capability. Instead, load the TXREGx register when the TRMT bit (TXSTAx<1>) is set, indicating the TSR is empty.

If double-buffering is used and back-to-back transmission is performed, load TXREGx immediately after TXxIF is set or wait 1-bit time after TXxIF is set. Both solutions prevent writing TXREGx while a Stop bit is transmitted. Note that TXxIF is set at the beginning of the Stop bit transmission.

If transmission is intermittent, do one of the following:

- Wait for the TRMT bit to be set before loading TXREGx.
- Execute the following:
  - Use a free timer resource to time the baud period.
  - Set up the timer to overflow at the end of Stop bit.
  - Start the timer when you load the TXREGx.
  - Do *not* load the TXREGx when the timer is about to overflow.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In 9-Bit Asynchronous Full-Duplex Receive mode, the received data may be corrupted if the TX9D bit (TXSTAx<0>) is not modified immediately after the RCIDL bit (BAUDCONx<6>) is set.

Work around

Write to TX9D only when a reception is not in progress (RCIDL = 1). Since there is no interrupt associated with RCIDL, it must be polled in software to determine when TX9D can be updated.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

After the last received byte has been read from the EUSART receive buffer (RCREGx), the value is no longer valid for subsequent read operations.

Work around

The RCREGx register should be read only once for each byte received. After each byte is received from the EUSART, store the byte into a user variable.

To determine when a byte is available to read from RCREGx, do one of the following:

- Poll the RCIDL bit (BAUDCONx<6>) for a low-to-high transition
- Use the EUSART Receive Interrupt Flag, RC1IF (PIR1<5>)

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

With the auto-wake-up option enabled by setting the WUE bit (BAUDCONx<1>), the RC1IF bit (PIR1<5>) will become set on a high-to-low transition on the RXx pin. While the WUE bit is set, reading the receive buffer (RCREGx) will not clear the RCxIF interrupt flag.

Because of this, RCxIF cannot be automatically cleared by reading RCREGx until the WUE bit is cleared.

Note:	RCxIF can only be cleared by reading RCREGx

Work around

Do the following:

1. Poll either the WUE bit or the RXx pin.
2. When WUE is clear or RXx is high, read RCREGx.

   Step 2 clears RCxIF.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: 10-Bit Analog-to-Digital (A/D) Converter

When the A/D conversion clock is selected to be either FOSC/64, FOSC/32 or FOSC/16, the GO/$\overline{\text{DONE}}$ bit cannot be set for a second conversion without first selecting (temporarily) the RC oscillator as the A/D conversion clock.

The A/D functions normally with the A/D conversion clock settings of FOSC/2, FOSC/4 and FRC.

Work around

For A/D conversion clock settings of FOSC/64, FOSC/32 or FOSC/16, perform the work around shown in Example 3 prior to setting the GO/$\overline{\text{DONE}}$ bit for subsequent conversions.

It is recommended that this code be inserted immediately after the A/D result has been read from the previous conversion.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 3:

```
MOVF    ADCON2, W          ;copy the value of ADCON2 to WREG
BSF     ADCON2, ADCS0      ;temporarily select RC oscillator as clock
BSF     ADCON2, ADCS1
MOVWF   ADCON2             ;restore ADCON2 to original value
```

16. Module: 10-Bit Analog-to-Digital (A/D) Converter

When FOSC/8 is selected as the A/D conversion clock, A/D conversion will not be performed.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (8/2007)

First release of this document. Includes silicon issues 1 (Flash Program Memory), 2-3 (External Memory Bus), 4 (Timer1), 5-10 (MSSP), 11-14 EUSART and 15-16 (10-Bit A/D Converter).

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06/25/07