International IOR Rectifier

IRDC3870

SupIRBuck™

USER GUIDE FOR IRDC3870 EVALUATION BOARD

DESCRIPTION

The IR3870 SupIRBuck™ is an easy-to-use, fully integrated and highly efficient DC/DC voltage regulator. The onboard constant on time hysteretic controller and MOSFETs make IR3870 a space-efficient solution that delivers up to 10A or precisely controlled output voltage in 60°C ambient temperature applications without airflow. It is housed in a in 20 Lead 5mmx6mm QFN package.

Key features offered by the IR3870 include: programmable switching frequency, soft start, and over current protection allows for a very flexible solution suitable for many different applications and an ideal choice for battery powered applications.

Additional features include pre-bias startup, very precise 0.5V reference, over/under voltage shut down, power good output, and enable input with voltage monitoring capability.

This user guide contains the schematic and bill of materials for the IRDC3870 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed specifications and application information for IR3870 is available in the IR3870 data sheet.

BOARD FEATURES

- V_{in} = +12V Typical (8-19V input Voltage range. see note below)
- PV_{cc}= +5.0V
- Vcc=+3.3V
- V_{out} = +1.1V @ 0- 10A
- F_s = 500kHz @ 10A
- L = 0.56uH
- C_{in}= 1x10uF (ceramic 1210) + 1x68uF (electrolytic)
- C_{out}= 2x10uF (ceramic 0805) + 1x150uF(SP Cap)

Note: At low input line an additional 10uF ceramic capacitor is recommended at input to handle higher ripple current)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN and PGND. A maximum 10A load should be connected to VOUT and PGND. The connection diagram is shown in Fig. 1 and inputs and outputs of the board are listed in Table I.

IRDC3870 has three input connectors, one for biasing (PVcc),one for biasing Vcc and the third one as input voltage (Vin). Separate supplies should be applied to these inputs. PVcc input should be a well regulated 4.5V-5.5V supply and it would be connected to PVcc and PGND and Vcc input should be a well regulated 3.0V-3.6V supply and it would be connected to Vcc and PGND. An external signal can be provided as Enable signal to turn on or turn off the converter. The absolute maximum voltage of Enable signal is +3.9V. A well regulated 0-2V signal source is used in this user guide.

The evaluation board is configured for use with 2x10uF (ceramic 0805) + 1x150uF (SP) capacitors. However, the design can be modified for an all ceramic output cap configuration by adding the inductor DCR sensing circuit as show in the schematic on page 8.

Table I. Connections

Connection	Signal Name
VIN (TP53)	VIN (+12V)
PGND (TP55)	Ground of VIN
PVcc+ (TP61)	PVcc input (+5.0V)
Vcc+ (TP59)	PVcc input (+3.3V)
PGND (TP62)	Ground for PVcc input
PGND (TP60)	Ground for Vcc input
VOUT (TB5)	V_{out} (+1.1V)
PGND (TB6)	Ground of V_{out}
Enable (TP52)	Enable input

LAYOUT

The PCB is a 4-layer board. All layers are 2 Oz. copper. The IR3870 and other components are mounted on the top and bottom side of the board.

Power supply decoupling capacitors, the Bootstrap capacitor and feedback components are located close to IR3870. The feedback resistors are connected to the output voltage at the point of regulation and are located close to IR3870. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

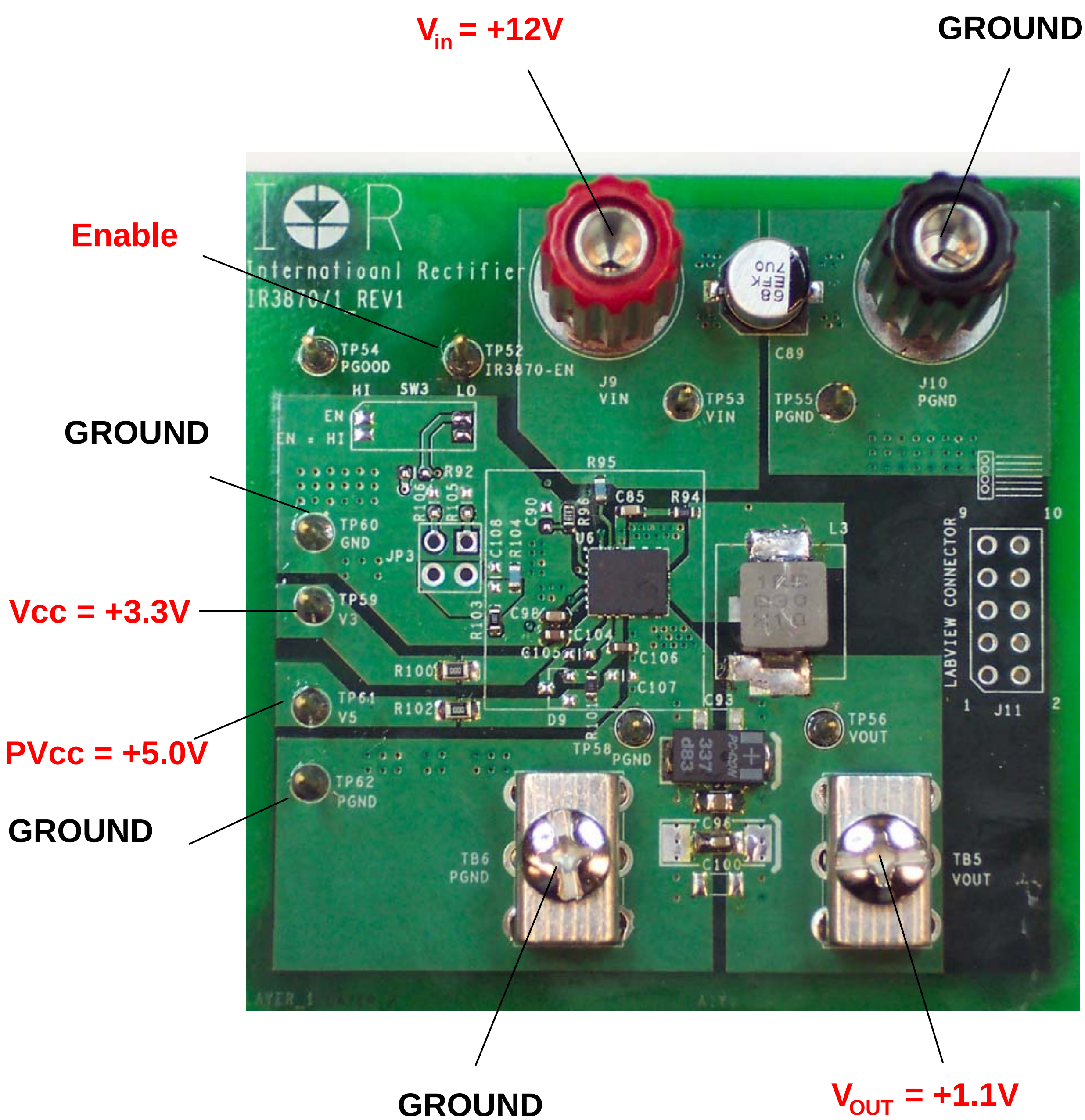


Fig. 1: Connection diagram of IRDC3870 evaluation board

PCB Board Layout

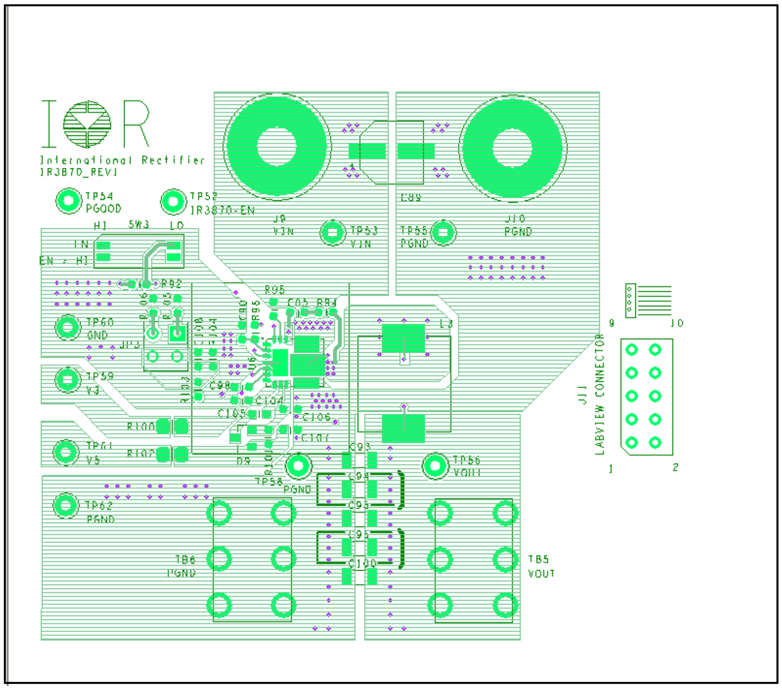


Fig. 2: Board layout, top layer

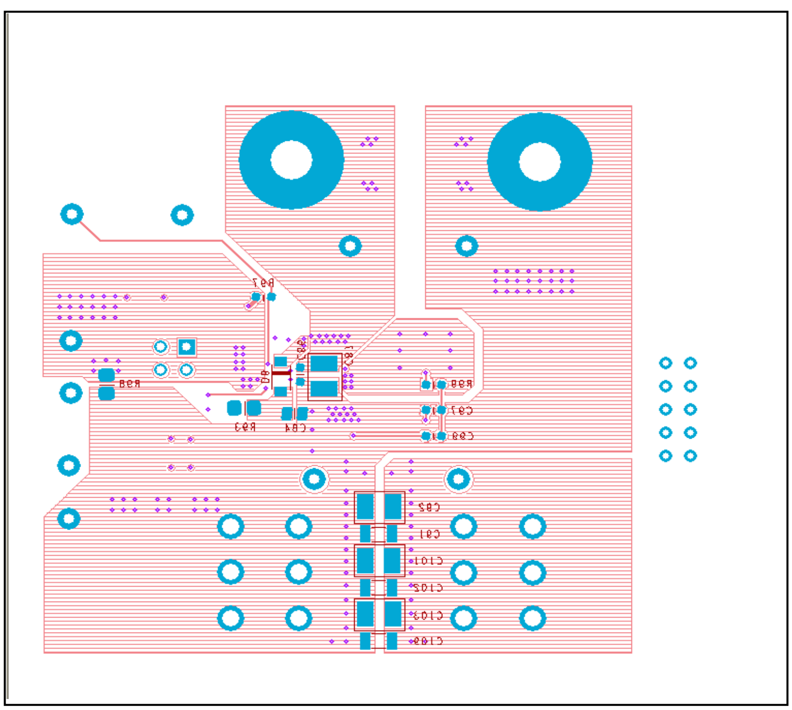


Fig. 3: Board layout, bottom layer

PCB Board Layout

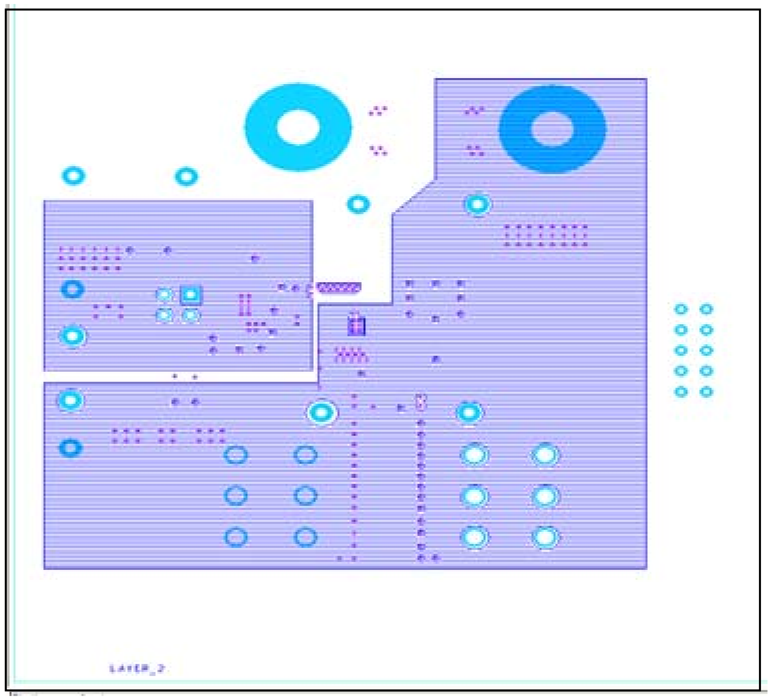


Fig. 4: Board layout, mid-layer I

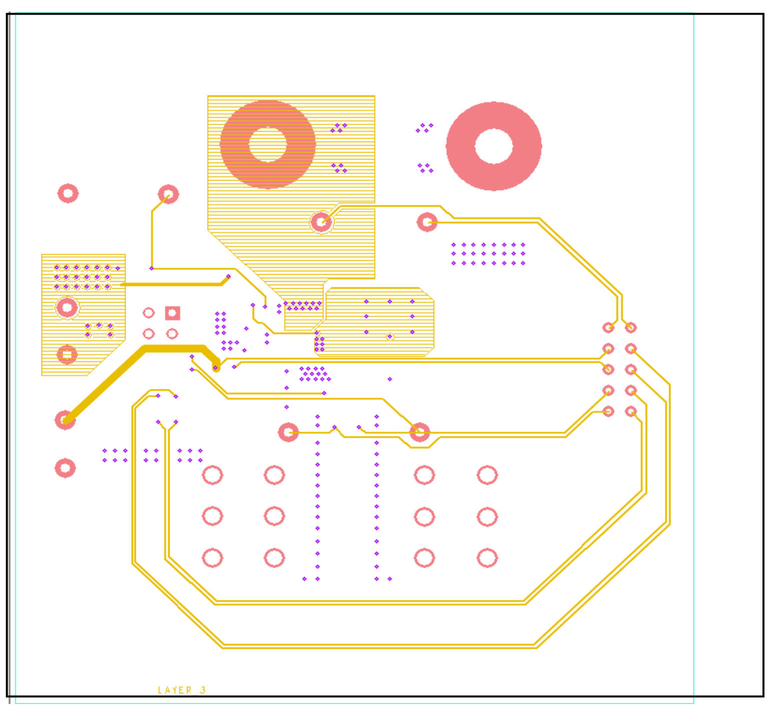


Fig. 5: Board layout, mid-layer II

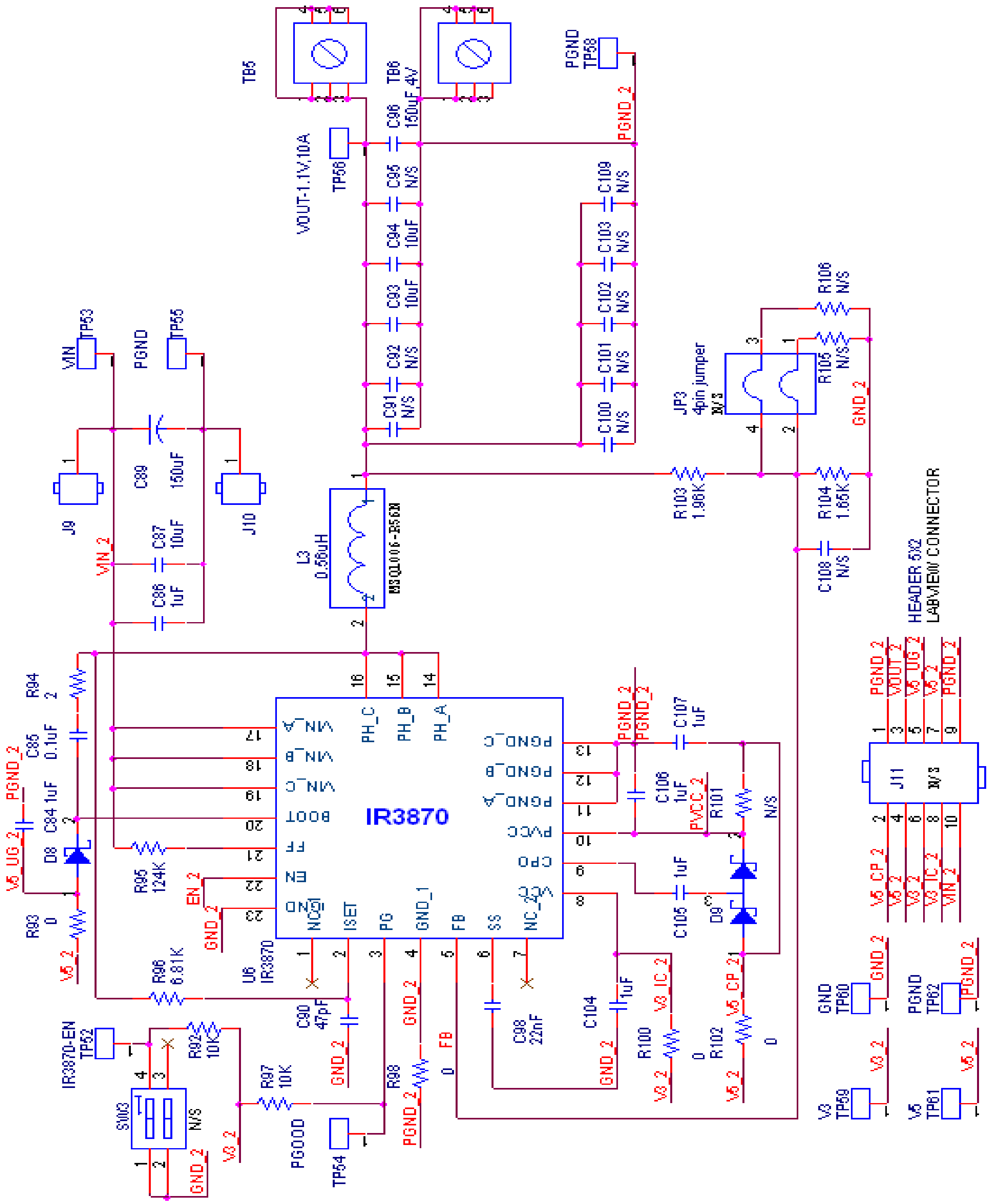


Fig.6: Schematic of the IRDC3870 evaluation board

Bill of Materials

Reference	Quantity	Value	Description	Part-Number	Manufacturer
C85	1	0.1uF	CAP,CER,0.1UF,50V,10%,X7R,0603	GRM188R71H104KA93D	Murata
C84,C86	2	1uF	CAP,CER,1.0UF,25V,X7R,0603	ECJ-3YB1E105K	Panasonic
C87	1	10uF	CAP,10UF,25V,CERAMIC,X5R,1210	ECJ-4YB1E106M	Panasonic
C89	1	150uF	CAP,150UF,35V,ELECT,FK,SMD	EEEFK1V101XP	Panasonic
C90	1	47pF	CAP,CER,47PF,50V,5%,C0G,0603	GRM1885C1H470JA01D	Murata
C96	1	150uF	CAP ,Polymer,150uF 4V	EEFCX0G151R	Panasonic
C92,C101,C103	3	DNI			
C93,C94	2	10uF	CAP,CER,10UF,6.3V,10%,X5R,0805	GRM21BR60J106KE19L	Murata
C98	1	22nF	CAP,CER,22000PF,50V,10%,X7R,0603	GRM188R71H223KA01D	Murata
C91,C95,C100,C102,C109	5	DNI		GRM31CF50J107ZE01L	Murata
C104,C105,C106,C107	4	1uF	CAP,CER,1.0UF,16V,X7R,0603	EMK107BJ105KA-TR	Taiyo Yuden
C108	1	DNI	CAP,1000PF,50V,CERAMIC,X7R,0603	C0603C102K5RACTU	kemet
D8	1	MBR0530	DIODE,SCHOTTKY,30V,0.5A,SOD123	MBR0530T1G	On Semiconductor
D9	1	BAT54S	DIODE,SCHOTTKY,30V,DUAL,SOT23	BAT54S-T/R	NXP Semiconductors
L3	1	0.56uH,4.0mOhm	SMT Power Inductor	MSQ1006-R56N-R	ACT
R92,R97	2	10K	RES,10.0K,OHM,1/10W,1%,0603,SMD	MCR03EZPFX1002	Rohm Semiconductor
R93,R98,R100,R102	4	0	RES,0.0,OHM,1/8W,5%,0805,SMD	MCR10EZPJ000	Rohm Semiconductor
R94	1	2	RES,2.00,OHM,1/10W,1%,0603,SMD	RC0603FR-072RL	AVX
R95	1	124K	RES,124,OHM,1/10W,1%,0603,SMD	RC0603FR-07124RL	AVX
R96	1	6.81K	RES,6.80K,OHM,1/10W,1%,0603,SMD	ERJ-3EKF6801V	Panasonic
R101	1	DNI			
R103	1	1.96k	RES,1.96K,OHM,1/10W,1%,0603,SMD	ERJ-3EKF1961V	Panasonic
R104	1	1.65K	RES,1.65K,OHM,1/10W,1%,0603,SMD	ERJ-3EKF1651V	Panasonic
R105,R106	2	DNI			
U6	1	IR3870			IR

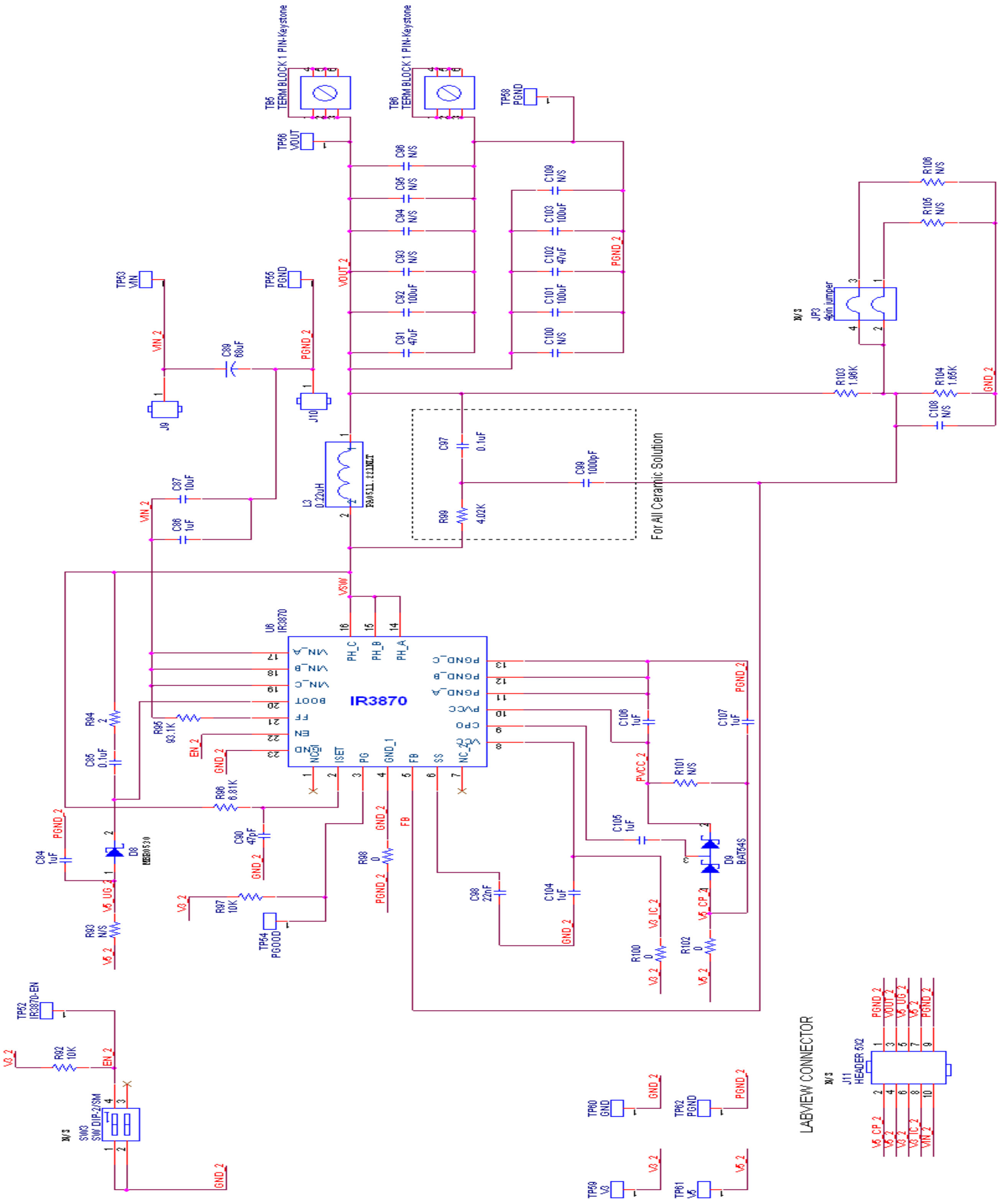


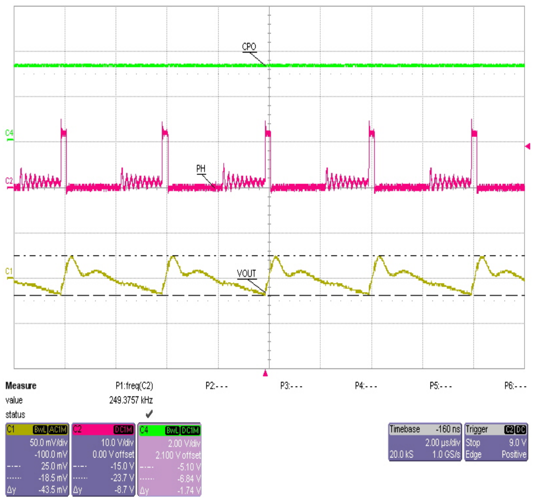
Fig.7: Schematic of the IRDC3870 using all Ceramic Output Capacitor

Bill of Materials with all Ceramic output Capacitors

Reference	Quantit y	Description	Part-Number	Manufacturer
C85,C97	2	CAP,CER,0.1uF,50V,10%,X7R,0603	GRM188R71H104KA93D	Murata
C84,C86	2	CAP,CER,1.0uF,25V,X7R,0603	ECJ-3YB1E105K	Panasonic
C87	1	CAP,10uF,25V,CERAMIC,X5R,1210	ECJ-4YB1E106M	Panasonic
C89	1	CAP,68uF,25V,ELECT,FK,SMD	EEV-FK1E680P	
C90	1	CAP,CER,47pF,50V,5%,C0G,0603	GRM1885C1H470JA01D	Murata
C93,C95,C100,C108	4	DNI		
C92,C101,C103	3	CAP,CER,100uF,6.3V,X5R,1210	C3225X5R0J107M	TDK
C94,C96,C109	3	DNI		
C98	1	CAP,CER,22000pF,50V,10%,X7R,0603	GRM188R71H223KA01D	Murata
C99	1	CAP,CER,1000pF,50V,5%,C0G,0603	GRM1885C1H102JA01D	Murata
C91,C102	2	CAP,CER,47uF,6.3V,X5R,0805	JMK212BJ476MG-T	Taiyo Yuden
C104,C105,C106,C107	4	CAP,CER,1.0uF,16V,X7R,0603	EMK107BJ105KA-TR	Taiyo Yuden
D8	1	DIODE,SCHOTTKY,30V,0.5A,SOD123	MBR0530T1G	On Semiconductor
D9	1	DIODE,SCHOTTKY,30V,DUAL,SOT23	BAT54S-T/R	NXP Semiconductor
L3	1	INDUCTOR,FERRITE,220nH,20%,25A,0.39mOhm,SMD	PA0511.221NLT	Pulse Engineering
R92,R97	2	RES,10.0K,OHM,1/10W,1%,0603,SMD	MCR03EZPFX1002	Rohm Semiconductor
R93,R98,R100,R102	4	RES,0.0,OHM,1/8W,5%,0805,SMD	MCR10EZPJ000	Rohm Semiconductor
R94	1	RES,2.00,OHM,1/10W,1%,0603,SMD	RC0603FR-072RL	AVX
R95	1	RES,93.1K,OHM,1/10W,1%,0603,SMD	CRCW060393K1FKEA	Vishay
R96	1	RES,6.80K,OHM,1/10W,1%,0603,SMD	ERJ-3EKF6801V	Panasonic
R99	1	RES,4.02K,OHM,1/10W,1%,0603,SMD	CRCW06034K02FKEA	Vishay
R101,R105,R106	3	DNI		
R103	1	RES,1.96K,OHM,1/10W,1%,0603,SMD	ERJ-3EKF1961V	Panasonic
R104	1	RES,1.65K,OHM,1/10W,1%,0603,SMD	ERJ-3EKF1651V	Panasonic
U6	1	IR3870		

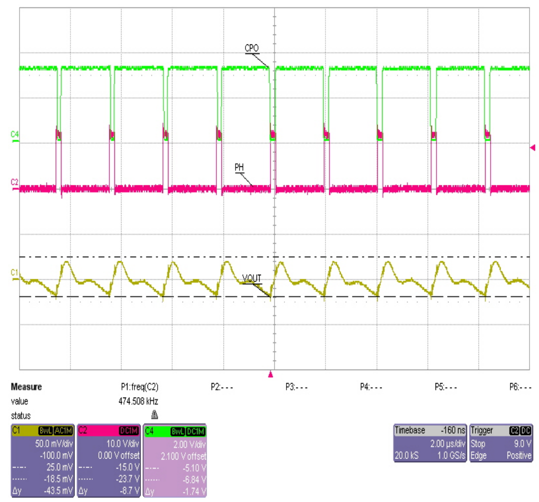
TYPICAL OPERATING WAVEFORMS

Vin=12V, PVcc=5.0V, Vcc=3.3V,Vo=1.1V, Io=0- 10A, , Room Temperature, No Air Flow



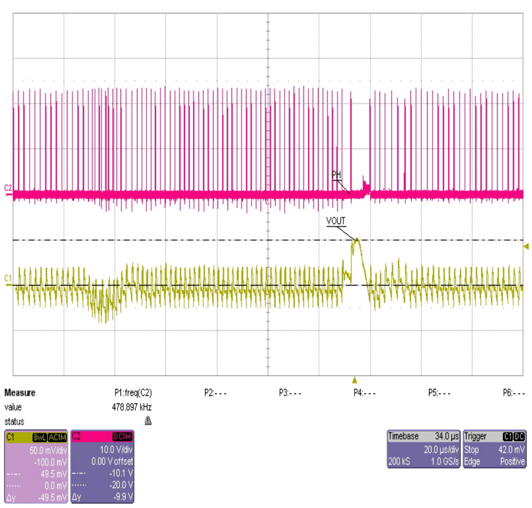
CH1: Vout (50mV/div); CH2: Phase (10V/div)
CH4: CPO (2V/div); Time: 2uS/div)

Figure 8: Charge Pump Off at Iout = 1A



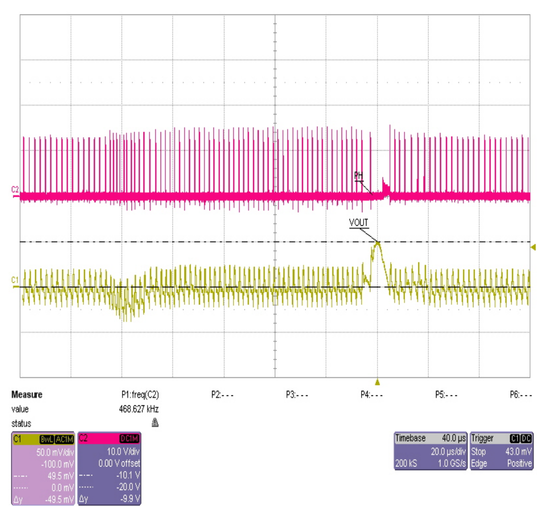
CH1: Vout (50mV/div); CH2: Phase (10V/div)
CH4: CPO (2V/div); Time: 2uS/div)

Figure 9: Charge Pump On at Iout =3A



CH1: Vout (50mV/div); 20uS/div
CH2: Phase (10V/div)

Figure 10: Load Step (2A to 10A) Transient (5A/uS) at 19Vin with 50mV Overshoot

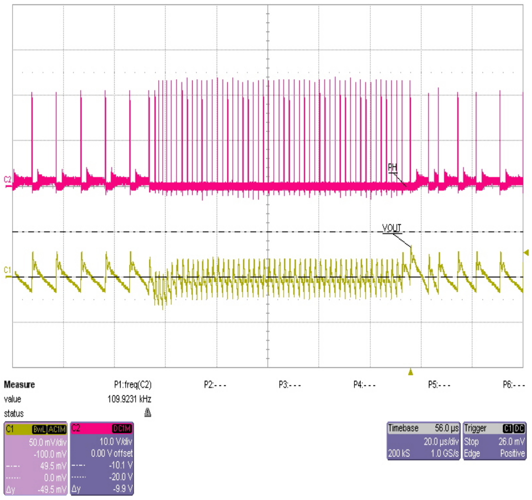


CH1: Vout (50mV/div); 20uS/div
CH2: Phase (10V/div)

Figure 11: Load Step (2A to 10A) Transient (5A/uS) at 12Vin with 50mV Overshoot

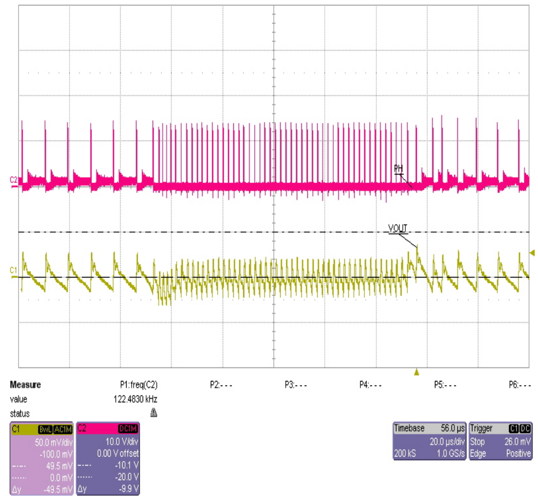
Note1: Enable is provided by an external signal (0-2.0V) after Vin=12V and PVcc=5.0V are applied.
Note2: Vo ripple is measured across the output capacitor.

TYPICAL OPERATING WAVEFORMS
Vin=12V, PVcc=5.0V, Vcc=3.3V,Vo=1.1V, Io=0- 10A, , Room Temperature, No Air Flow



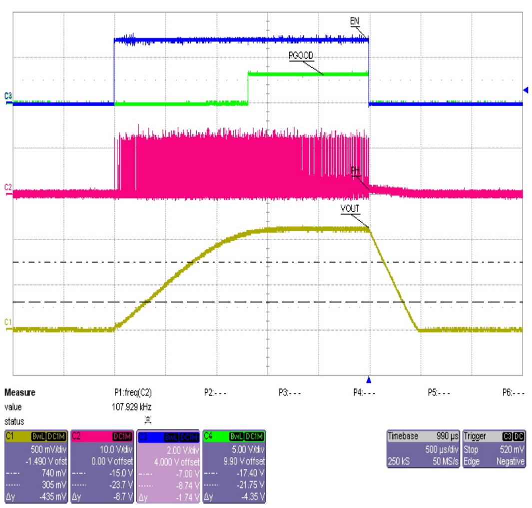
CH1: Vout (50mV/div); 20uS/div
CH2: PHASE (10V/div)

Figure 12: FCCM/CCM transition from 0.5A to 5A at 19Vin



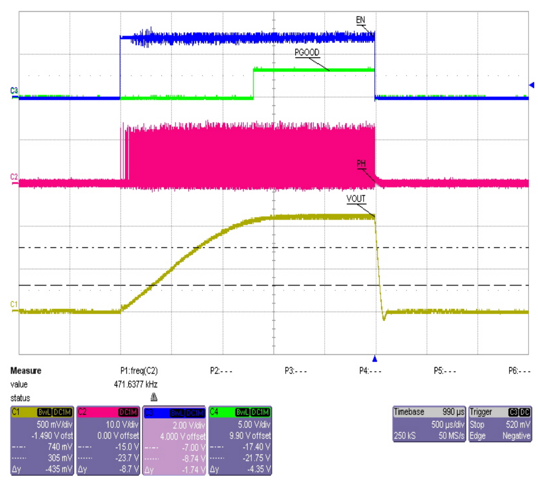
CH1: Vout (50mV/div); 20uS/div
CH2: PHASE (10V/div)

Figure 13: FCCM/CCM transition from 0.5A to 5A at 12Vin



CH1: Vout (500mV/div); 500uS/div
CH2: PHASE (10V/div)
CH3: EN (2V/div)
CH4: PGOOD (5V/div)

Figure 14: Startup/Shutdown 12Vin at 500mA



CH1: Vout (500mV/div); 500uS/div
CH2: PHASE (10V/div)
CH3: EN (2V/div)
CH4: PGOOD (5V/div)

Figure 15: Startup/Shutdown 12Vin at 3A

TYPICAL OPERATING WAVEFORMS

Vin=12V, PVcc=5.0V, Vcc=3.3V, Vo=1.1V, Io=0- 10A, , Room Temperature, No Air Flow

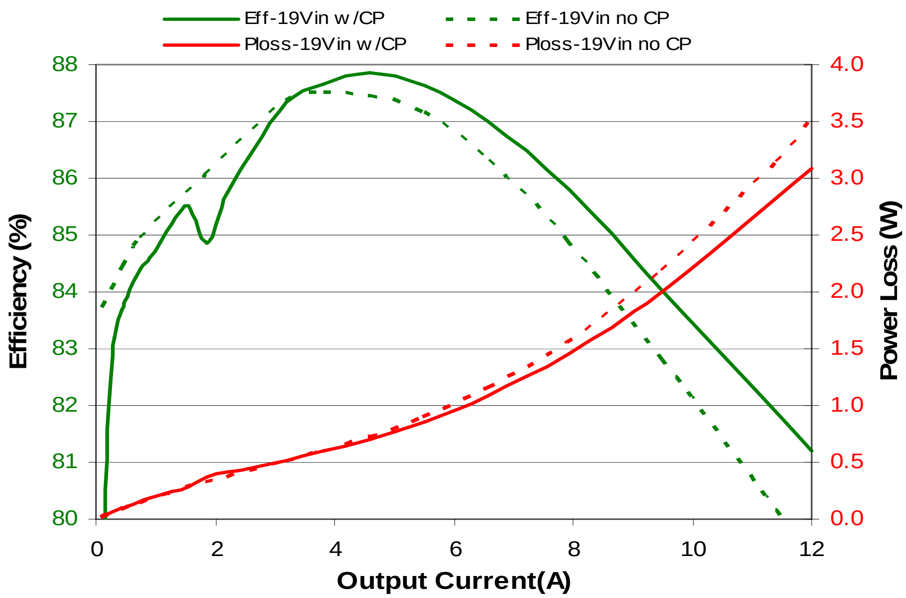


Figure 16: Typical Efficiency and Power Loss of Converter Vout = 1.1V

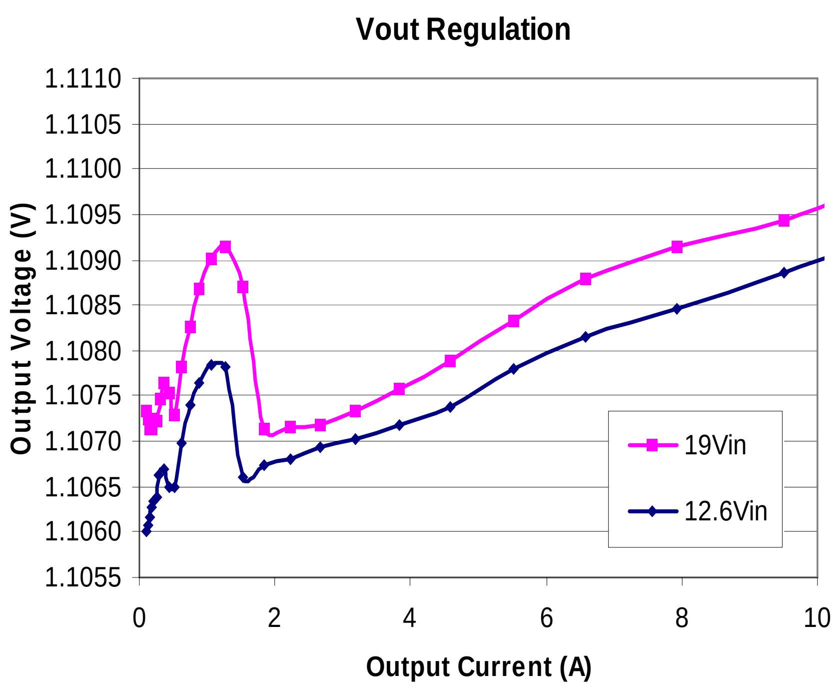
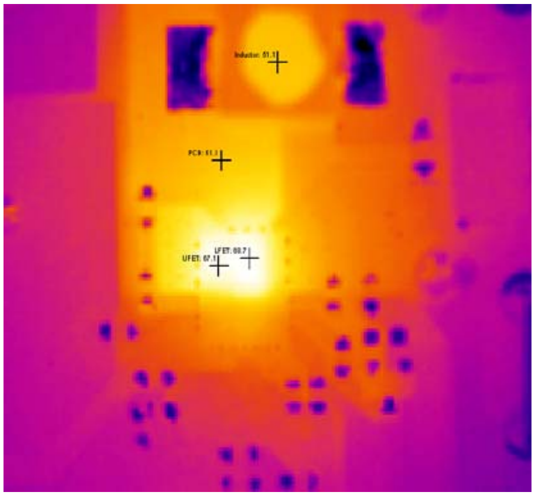


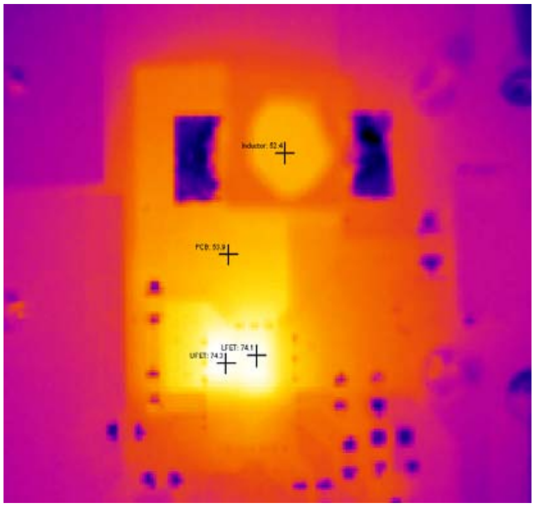
Figure 17: Typical Output Voltage Regulation

TYPICAL OPERATING WAVEFORMS
Vin=12V, PVcc=5.0V, Vcc=3.3V, Vo=1.1V, Io=0- 10A, , Room Temperature, No Air Flow



IC: 69°C, Inductor: 51°C, PCB: 51°C

Figure 18: Thermal Image @12Vin, 10A, Ta= 25°C and no air flow



IC: 75°C, Inductor: 53°C, PCB: 54°C

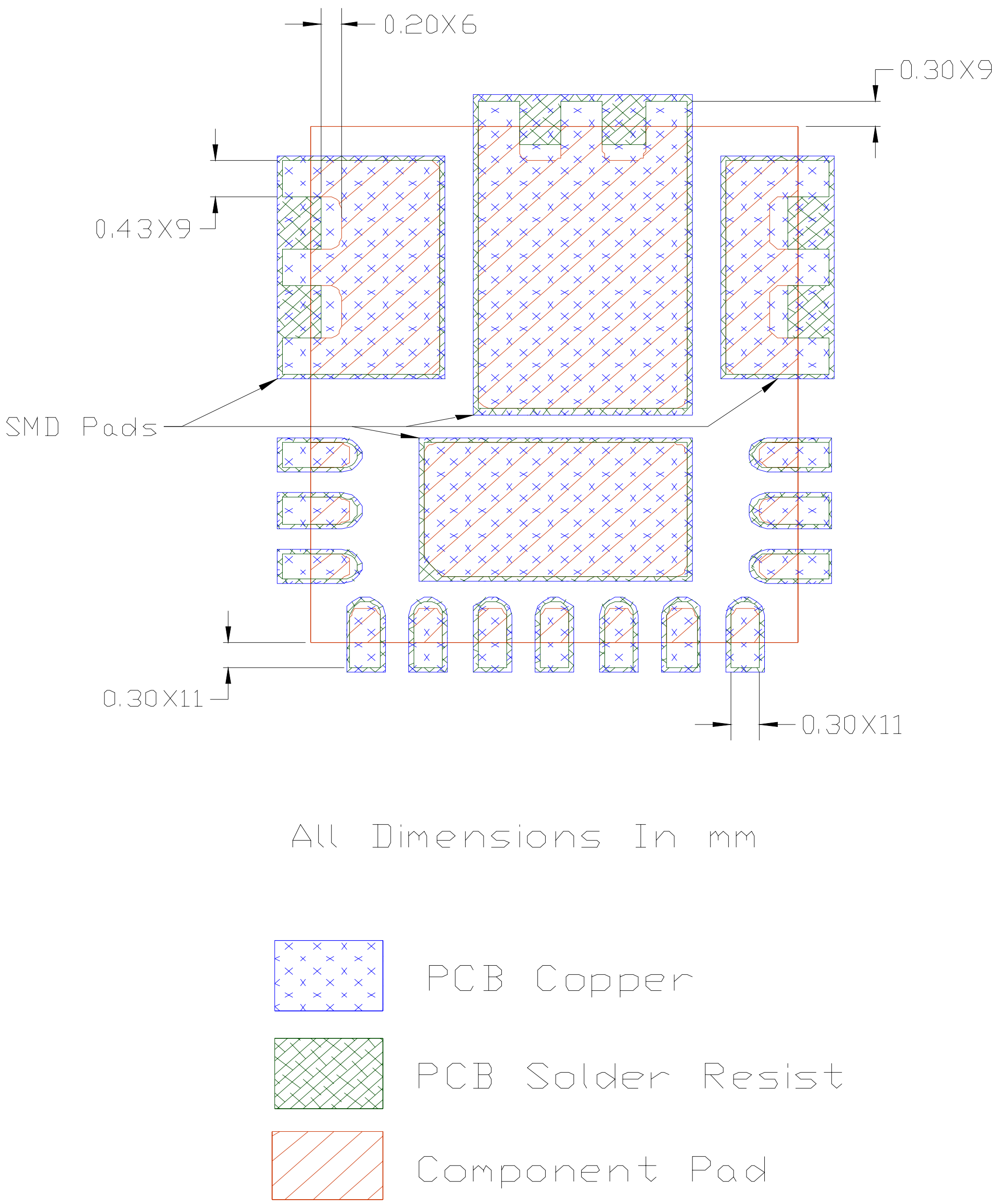
Figure 19: Thermal Image @19Vin, 10A, Ta= 25°C and no air flow

PCB Metal and Components Placement

Lead lands (the 13 IC pins) width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.

Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension. The outboard extension ensures a large toe fillet that can be easily inspected.

Pad lands (the 4 big pads) length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be no less than; 0.17mm for 2 oz. Copper or no less than 0.1mm for 1 oz. Copper or no less than 0.23mm for 3 oz. Copper.

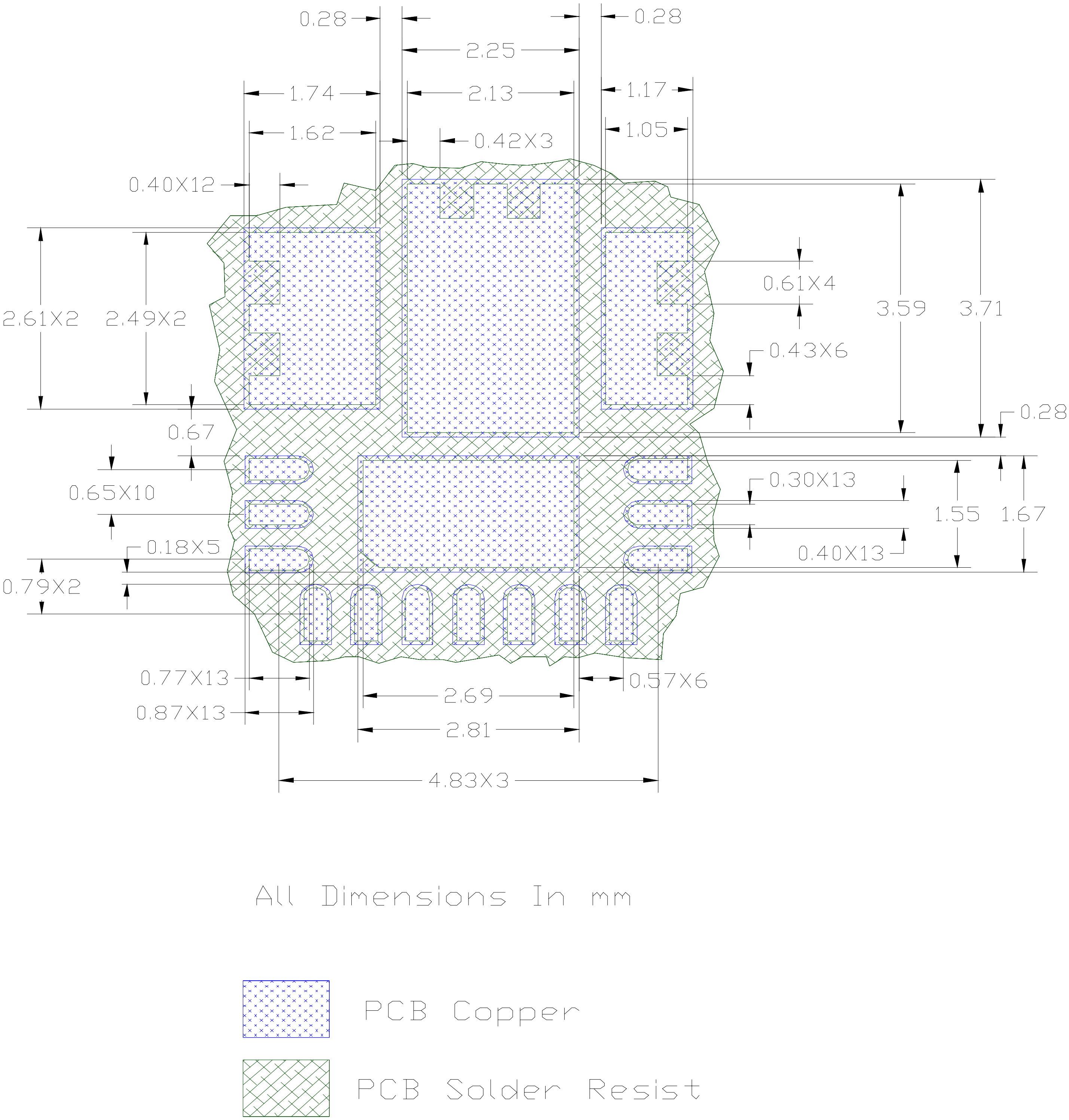


Solder Resist

It is recommended that the lead lands are Non Solder Mask Defined (NSMD). The solder resist should be pulled away from the metal lead lands by a minimum of 0.025mm to ensure NSMD pads.

The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.05mm to accommodate solder resist misalignment.

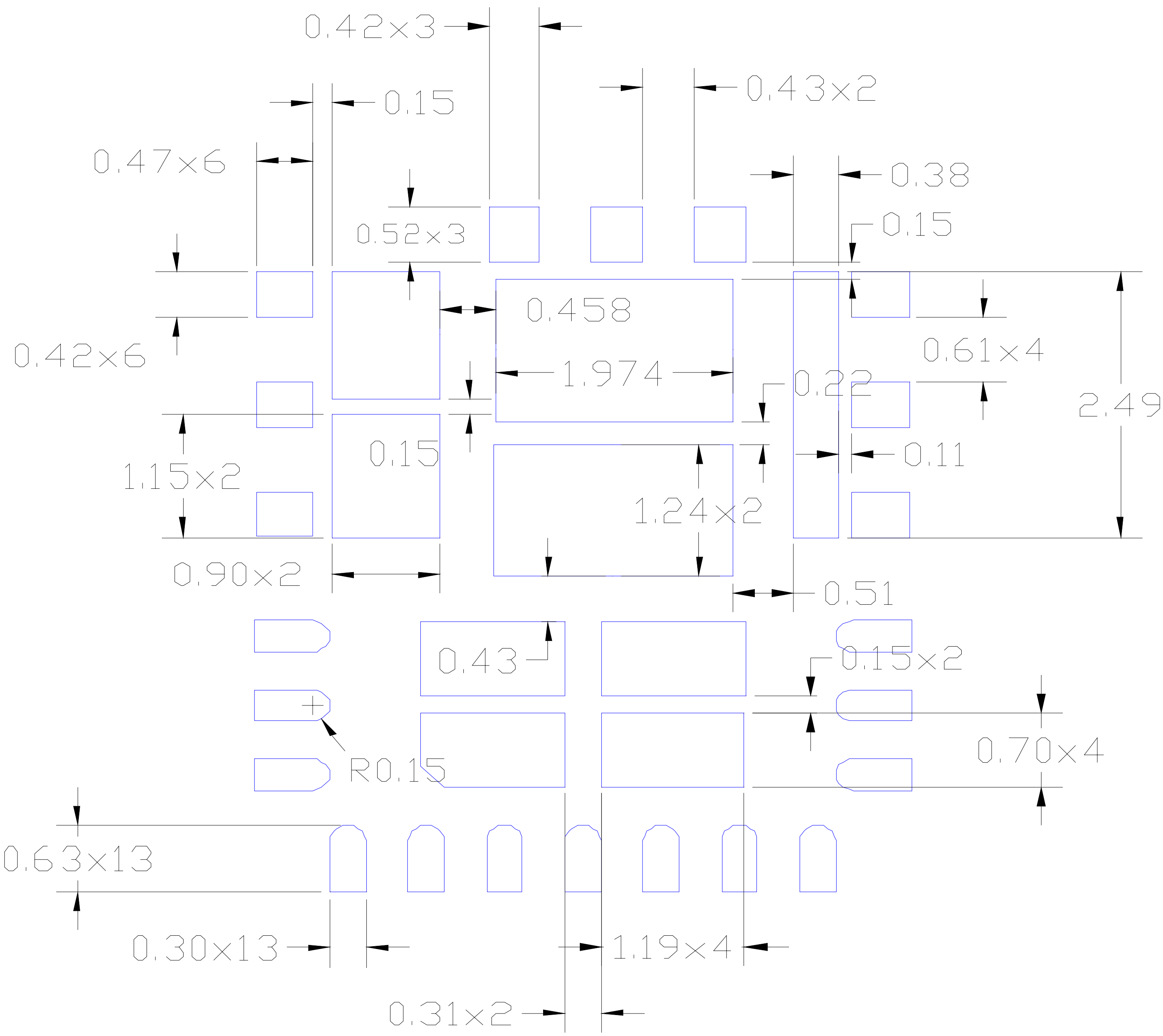
Ensure that the solder resist in between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.



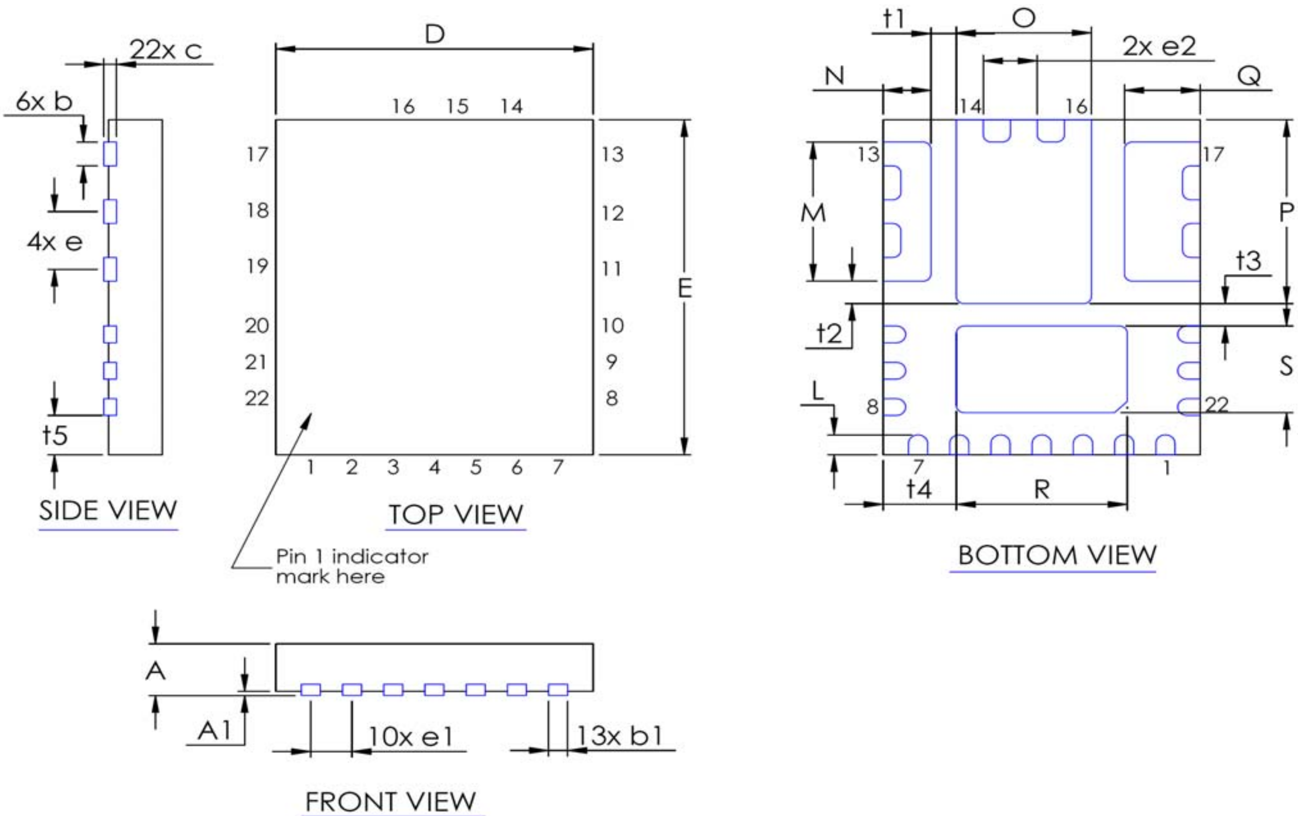
Stencil Design

The Stencil apertures for the lead lands should be approximately 80% of the area of the lead lads. Reducing the amount of solder deposited will minimize the occurrences of lead shorts. If too much solder is deposited on the center pad the part will float and the lead lands will open.

The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back in order to decrease the risk of shorting the center land to the lead lands when the part is pushed into the solder paste.



Mechanical Outline Drawing



DIM	MILIMITERS		INCHES		DIM	MILIMITERS		INCHES	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.8	1	0.0315	0.0394	L	0.35	0.45	0.0138	0.0177
A1	0	0.05	0	0.002	M	2.441	2.541	0.0962	0.1001
b	0.375	0.475	0.1477	0.1871	N	0.703	0.803	0.0277	0.0314
b1	0.25	0.35	0.0098	0.1379	O	2.079	2.179	0.0819	0.0858
c	0.203 REF.		0.008 REF.		P	3.242	3.342	0.1276	0.1316
D	5.000 BASIC		1.970 BASIC		Q	1.265	1.365	0.0498	0.05374
E	6.000 BASIC		2.364 BASIC		R	2.644	2.744	0.1042	0.1081
e	1.033 BASIC		0.0407 BASIC		S	1.5	1.6	0.0591	0.063
e1	0.650 BASIC		0.0256 BASIC		t1, t2, t3	0.401 BASIC		0.016 BACIS	
e2	0.852 BASIC		0.0259 BASIC		t4	1.153 BASIC		0.045 BASIC	
					t5	0.727 BASIC		0.0286 BASIC	

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