User's Manual

RZ/G1E

User's Manual: Hardware

for Rich Graphics Applications
RZ/G Series

ARM®

Specifications of Individual RZ/G Series Product

Renesas Electronics
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(2012.4)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of hardware, pin assignments, pin multiplexing, and pin function controller.

For the rest of the sections on other on-chip peripheral functions, see the RZ/G Series User's Manual: Hardware.

> Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

> The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

We provide the following three types of user's manual for RZ/G Series products.

Make sure to refer to the latest versions of these documents.

Document Type	Description	Document Title	Document No.
User's manual for specifications of individual RZ/G Series product	Overview of hardware, pin assignments, pin multiplexing, and pin function controller	RZ/G1E User's Manual: Hardware	R01UH0544EJ0100 Rev.1.00 (This user's manual)
User's manual for specifications common to RZ/G Series products	Hardware specifications (address map, general-purpose I/O port pins, clock, reset, core functions, graphics, video processing, sound processing, and network modules, serial interfaces, storage, timers, other on-chip peripheral functions, testing, and debugging) and descriptions of operation	RZ/G Series User's Manual: Hardware	R01UH0543EJ0100 Rev.1.00
User's manual for electrical characteristics	Electrical characteristics of the RZ/G Series products	Provided as separate technical information.	

2. Notation of Numbers and Symbols

Bit notation: Bits are shown in high-to-low order from left to right.

Number notation: Binary numbers are given as B'XXXX, hexadecimal numbers are given as H'XXXX, and decimal numbers are given as XXXX.

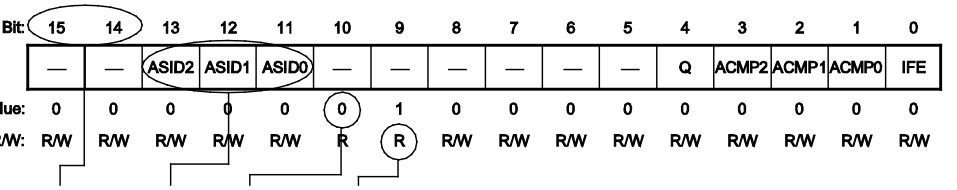
Signal notation: A number sign (#) after the name indicates that a signal or pin is active-low, unless otherwise specified.

Example: PRESET#

3. Register Notation

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings.

[Bit Chart]



[Table of Bits]

(1) (2) (3) (4) (5)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved
14	—	0	R	These bits are always read as 0.
13 to 11	ASID2 to ASID0	All 0	R/W	Address Identifier These bits enable or disable the pin function.
10	—	0	R	Reserved This bit is always read as 0.
9	—	1	R	Reserved This bit is always read as 1.
	—	0		

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

(1) Bit
Indicates the bit number or numbers.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

(2) Bit name
Indicates the name of the bit or bit field.
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).
A reserved bit is indicated by "–".
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

(3) Initial value
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
0: The initial value is 0.
1: The initial value is 1.
–: The initial value is undefined

(4) R/W
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.
The notation is as follows:

R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable.
However, writing is only performed to flag clearing.
R/WC0: The bit or field is readable and writable. Writing 0 to the bit initializes the bit.
Writing 1 to the bit is ignored.
R/WC1: The bit or field is readable and writable. Writing 1 to the bit initializes the bit.
Writing 0 to the bit is ignored.
R: The bit or field is readable.
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.
W: The bit or field is writable.
Note that values read from write-only bits are not guaranteed, unless they are specified in the chart of bits.

(5) Description
Describes the function of the bit or field and specifies the values for writing.

Contents

1. Overview

1.1 Introduction

The RZ/G1E is that features the basic functions for Rich Graphics Applications.

The RZ/G1E includes:

- Two 1.0-GHz ARM Cortex®-A7 MPCore® cores,
- Memory controller for DDR3-SDRAM (DDR3-1333) with 32 bits × 1 channel,
- Three-dimensional graphics engines,
- Video processing unit,
- 2 channels Display Output,
- 2 channels Video Input,
- Sound processing unit,
- SD card host interface,
- USB2.0 interfaces, and
- CAN interface.

Also, a full implementation of the extremely expandable and Internal AXI bus has been adopted for the RZ/G1E.

This bus structure is optimized for maximum system performance, leading to the realization of high-performance and cost-effective premium in-vehicle infotainment systems.

Notes: 1. ARM is a registered trademark and Cortex is a trademark of ARM Limited. All other brands or product names are the property of their respective holders.

1.2 System Configuration Diagram

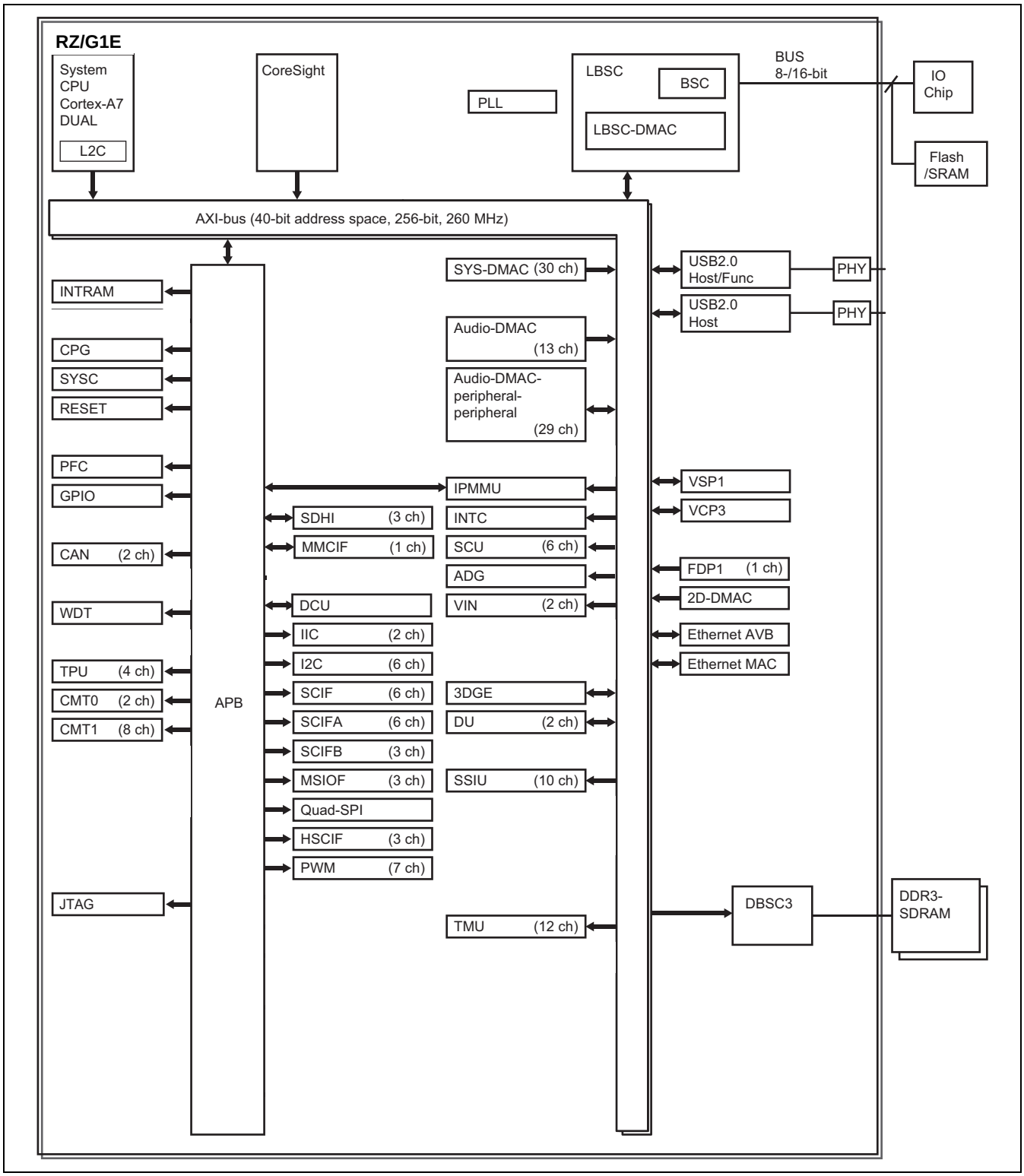


Figure 1.1 RZ/G1E System Configuration

1.3 List of Specifications

1.3.1 ARM Core

Item	Description
System CPU Cortex-A7	• ARM Cortex-A7 Dual MPCore 1.0 GHz • L1 I/D cache 32/32 KBytes, L2 cache 512 KBytes • NEON™/VFPv4 supported • Security extension supported
ARM debugger (CoreSight™)	• CoreSight system compliant • JTAG/SWD I/F supported • CoreSight ETR 16 KBytes for program flow trace • CoreSight ETR 4 KBytes for system trace

1.3.2 CPU Core Peripherals

Item	Description
Operating clock pulse generation circuit (CPG)	• Generates the clocks from external clock (EXTAL). — Maximum Cortex-A7 clock: 1.0 GHz — Maximum AXI-bus clock: 260 MHz — Maximum SDRAM bus clock: DDR3-1333 — Maximum media clock: 260 MHz — Maximum peripheral clock (HPϕ): 130 MHz • Module-standby mode supported • Includes module reset registers to control reset operation of individual on-chip peripheral modules
Reset (RESET)	• Includes one reset-signal external output port for external modules • Includes Boot Address Register etc.
Pin function controller (PFC)	• Setting multiplexed pin functions for LSI pins Function of the RZ/G1E pin selectable by setting the registers in the PFC module • Module selection Enable and disable the functions of RZ/G1E LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module. • Pull-up control for each LSI pin On/off of the pull-up resistor on each LSI pin can be controlled by setting the registers in the PFC module. • Control of SDIO functions SDIO functions, including the driving ability of pins for the SDIF, can be controlled by setting registers of the PFC
General-purpose I/O (GPIO)	• General-purpose I/O ports: 208 ports • Supports GPIO interrupts.

1.3.3 External Bus Module

Item	Description
Local bus state controller (LBSC)	• EX-BUS interface: max. 16-bit bus • Frequency: 65 MHz • External area divided into several areas and managed — Allocation to space of area 0, area 1, and area 6 or allocation to space of area 0 only is selected at startup time. — Area 0 supports 128-MByte memory space (startup mode). — Space of area 6 is divided into up to six areas (capacity of each area variable) and managed — I/F settings, bus width settings, and wait state insertion are possible for each area • SRAM interface — Wait states can be inserted through register settings Period of waiting is set in cycle unit, and the maximum value is 15. — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • Burst ROM interface — Wait states can be inserted through register settings — Number of bursts can be set through register settings — Connectable bus widths: 16 bits or 8 bits • Byte-control SRAM interface (available with areas 1 and 6 only) — Byte-control SRAM interface — Wait states can be inserted through register settings — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • ATA interface (two ports) — Wait states can be inserted through register settings — Supports PIO modes 0 through 4 — Supports multi-word modes 0 through 2 — Supports Ultra DMA modes 0 through 4 (Ultra ATA66) — Ready timeout detection (detection time (ns) = EX-BUS operating frequency (ns) × 100 clock cycles) • Supports external buffer enable/direction control

Item	Description
LBSC-DMAC	• Number of channels: LBSC-DMAC three channels • Address space: Physical address space • Transfer direction: Peripheral to memory (AXI-bus), memory (AXI-bus) to peripheral • Data packing for peripheral read data: Memory write data length is selectable as transfer data length to memory side. • Transfer data length: Peripheral (APB-bus) side : 1, 2, 4 bytes Memory (AXI-bus) side : 4 or 16 (channel 2), 32 (channel 0 and 1) bytes • Transfer burst length: 1, 8 (transfer with a burst length of 8 supported only for LBSCDMAC00, 01) • Number of transfers — Maximum number of transfers: 16 M (16,777,216 transfers), 64M (67,108,864 transfers), (64 M transfers supported only for LBSC-DMAC00) — Minimum number of transfers: One • Address mode: Dual address mode • Transfer modes: Single transfer mode, continuous transfer mode • Transfer end interrupt: Occurs at the end of the number of transfers specified in the register
DDR3-SDRAM bus state controller (DBSC)	• 1 channel (32-bit bus) • DDR3-SDRAM can be connected directly. • Memory Size: Up to 2 GB (8-Gbit memory × 2) • Data bus width: 32 bits × 1 • Auto Refresh/Self Refresh/Partial Array Self Refresh supported • Deep-Power-Down-Mode supported • Auto Pre-charge Mode/Bank Active Mode • DDR Back Up supported
Memory connections	DDR3-SDRAM compliant to JEDEC JESD79-3E Supports from 512-Mbit to 8-Gbit memory unit configurations 32-bit DDR3-1333 (four units with 8-bit width)

1.3.4 Internal Bus Module

Item	Description
AXI-bus	• On-chip main bus — Bus protocol : AXI3 with QoS control — Frequency: 260 MHz — Bus width: 256 bits/128 bits • On-chip CPU & GPU main bus — Corelink™ CCI-400 Cache Coherent Interconnect - r0p3 — Bus protocol: AMBA®4 ACE™ and ACE-Lite™ — Frequency: 520 MHz — Bus width: 128 bits
Direct memory access controller (SYS-DMAC)	• 30 channels for ARM domain • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Direct memory access controller (Audio-DMAC)	• 13 channels for Audio domain • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)

Item	Description	
Direct memory access controller (Audio-DMAC-Peripheral-Peripheral)	Audio-DMAC (for transfer from Peripheral to Peripheral) • 29 channels for audio domain • Data transfer length: longword (4 Bytes) • Transfer count: Transfer count is not specified (DMA transfer is made from the transfer-start to transfer-stop settings.) • Transfer request: Selectable from on-chip audio peripheral module request • Priority: round-robin mode • Interrupt request: not supports interrupt request to CPU at the end of data transfer	
IPMMU	An IPMMU is a memory management unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.	
Interrupt controller (INTC)	INTC-SYS	— 10 interrupt pins which can detect external interrupts — Fall/rise/high level/low level detection is selectable — On-chip peripheral interrupts: Priority can be specified for each module — Max. 384 shared peripheral interrupts supported — 16 software interrupts that have been generated and 6 private peripheral interrupts supported — 32-level priority selectable — Trust Zone supported

1.3.5 Local Memory

Item	Description
INTRAM	• RAM0 of 72 KBytes • RAM1 of 4 KBytes • RAM2 of 256 KBytes

1.3.6 Graphics Units

Item	Description	
3D graphics engine (3DGE)	• Imagination Technologies PowerVR Series5 SGX540 (260 MHz) • USSE2 delivers twice the peak floating point and instruction throughput of Series5 USSE • YCbCr and color space accelerators for improved performance • Upgraded PowerVR Series5XT shader-driven tile-based deferred rendering (TBDR) architecture • Support for all industry standard mobile and desktop graphics APIs and operating systems	
Display unit (DU)	Screen size and number of composite planes	• Maximum screen size: 4095 × 2047 • Number of planes specifiable: 1 (ARGB8888)
	CRT scanning method	Non-interlaced, interlaced sync, interlaced sync & video
	Synchronization method	Master, TV sync
	Internal color palette	Includes four color palette planes which can display 256 of 260 thousands colors at the same time.
	Digital RGB	• Two output channel • Output on rising and falling edges of the synchronizing signal (resolution for the same display) • 8-bit precision for each RGB color
	Blending ratio settings	Number of color palette planes with blending ratio: 4
	Dot clock	Switchable between external input and internal clock
	Color management	• γ correction, gain correction • Applies correction of color (skin color adjustment and color correction set in memory) in terms of color phase, brightness, and chromaticity for a specified range of colors or for the full range of colors
	Interface	• RGB888 × 2
De-Compression Unit(DCU)	• De-compression to row picture data from compressed data by Run-length method • Input data format: Compressed data by Run-Length method (ARGB8888, RGB888, RGB565, RGBA4444, RGBA5551, and A8) • Output data format: Row data (ARGB8888, RGB888, RGB565, RGBA4444, RGBA5551, and A8) • 2 interrupt sources: Conversion finished, and Check sum error • Including DMAC (DCU_DMAC)	

Item	Description	
Video input (VIN)	Input data format	• 8-, 10-, or 12-bit YCbCr422 (CbYCrY format) • 16-bit YCbCr422 (8 bits (Y) + 8 bits (CbCr) format) • 20-bit YCbCr422 (10 bits (Y) + 10 bits (CbCr) format) • 24-bit YCbCr422 (12 bits (Y) + 12 bits (CbCr) format) • 18-bit RGB666 • 24-bit RGB888
	Clipping function	Up to 2048 × 2048
	Horizontal scaling	Uses a 9-tap multi-phase filter. Up to two times, but only scaling down is possible for HD1080i or HD720P data.
	Vertical scaling	Scaling by linear interpolation Up to three times, but only scaling down is possible for HD1080i or HD720P data.
	Output format	RGB-565, ARGB-1555, YCbCr422, RGB888 (channel 0,1), YC separation, and extraction of the Y component

1.3.7 Video Processing

Item	Description
Video signal processor 1 (VSP1)	The VSP1 is the successor IP of Renesas' VIO6-IP series, and has the following features. (1) Supports Various Data Formats and Conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying (2) Full HD Video Processing — Up and down scaling with arbitrary scaling ratio — Super resolution processing — Blending of four picture layers and raster operations (ROPs) (3) Full HD Picture Quality/Color Correction with 1D/3D Look Up Table(LUT) — Dynamic γ correction and gain correction — Correction of color (to adjust skin tones or colors in memory) — Hue, brightness, and saturation adjustment — 1D histogram (4) Direct Connection to Display Module — Display unit (DU) supported

Item	Description
Video processing unit (VCP3)	The VCP3 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.264/AVC, MPEG-4, MPEG-2 and VC-1. This IP (Intellectual Property) is a multi codec that processes the frame or each field by controlling software for VCP3 executed on host CPU. The VCP3 has the following features: • Support for multiple codecs H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding H.262/MPEG-2 MP (Main Profile) decoding MPEG-4 ASP (Advanced Simple Profile) decoding VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding H.263 Baseline decoding AVS Jizhun Profile decoding VP8 decoding • Support for HDTV resolutions 1920 pixels × 1080 lines × 60 frames/second × 1 channel Maximum performance will change with securable bus bandwidth. • Data handling on a picture-by-picture basis Encodes/decodes data one picture (frame or field) at a time. • High picture quality Supports the H.264 high-efficiency coding tools (CABAC, 8 × 8 frequency conversion, and quantization matrix). High-efficiency motion vector detection by a combination of discrete search and trace search Highly efficient real-time intra-prediction by Prediction from Original Image (POI) Optimal-mode selection by Rate-Distortion (RD) cost evaluation Picture quality control based on activity analysis results which match visual models • Low power dissipation Dynamically disables the clocks for the entire VCP3. Dynamically disables the clocks for individual submodules. • Includes its own dedicated 64-KByte cache
Fine display processor 1 (FDP1)	The FDP1 is the de-interlacing module which converts the interlaced video to progressive video, and has the following features. (1) Supports various data formats — Input: YCbCr444/422/420 — Output: YCbCr444/422/420 and RGB/αRGB (2) Full HD video processing performance (3) High image quality de-interlacing algorithm — Motion adaptive de-interlacing — Accurate still detection — Diagonal line interpolation (DLI)

Item	Description
2-dimensional DMAC (2D-DMAC)	• Supports conversion between various RGB formats. • Image extraction function: Capable of extracting an image and storing it as a separate image in the RAM. • Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270°. • Simple scaling function: Capable of scaling an image two times in the X or Y direction. • Format conversion • Supports conversion from RGB to RGB and from YCbCr to YCbCr.

1.3.8 Sound Interface

Item	Description	
Sampling rate converter unit (SCU)	Overall specification	• Includes six SRC modules — Supports the quality suitable for audio sound (THD+N -132dB) : four modules — Supports the quality suitable for voice sound (THD+N -96dB) : two modules • The SRC module is capable of correcting phase change and delay (timing jitter) generated during data transfer over external memories or external devices. • The channel count conversion unit (CTU), mixer (MIX), and digital mute and volume function (DVC) can be used on two fixed output channels.
	Sampling rate conversion (SRC)	• Capable of asynchronous sampling rate conversion • Supports resolutions up to 24 bits • Two kinds of filter type for SRC. — Supports the quality suitable for audio sound (THD+N -132dB) : Realized the filter by passband -1dB@0.4575FS, cutoff -18dB@0.5FS. — Supports the quality suitable for voice sound (THD+N -96dB) : Realized the filter by passband -1dB@0.4561FS, cutoff -72dB@0.5FS. (Characteristics of each filter is written in the equivalent/up-sampling cases.) • Automatically generates antialiasing filter coefficients • For monaural to eight-channel sound sources
	Channel count conversion unit (CTU)	• Downmixing and splitter functions — Conversion of eight input channels into four output channels — Conversion of six input channels into two output channels — Conversion of two input channels into four sets of two output channels — Conversion of one input channel into eight sets of one output channel — No conversion
	Mixer (MIX)	• Mixing (adds) two to four sources into one • Ratio for adding sources is selectable • Ratio is dynamically changeable • Mixing with volume ramp is available (ramp period is selectable)
	Digital volume and mute function (DVC)	• Volume control function including digital volume, volume ramp, and zero-crossing mute • The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute, or -120 to 18 dB) • The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment • The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2 • The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

Item	Description	
Serial sound interface unit (SSIU)	Overall specification	• Includes ten SSI modules functioning as interfaces with external devices. — Supports short and long formats — Supports TDM format (six modules of ten modules can be used for this function) • Max. 4 independent stereo sound sources in a TDM format can be distributed to each course. Moreover Max. 4 independent stereo sound source can be combined output in TDM format.
	Serial sound interface (SSI)	• Operating mode: non-compressed mode (Not support compressed mode) • Supports versatile serial audio formats (I2S/left justified/right justified) • Supports master/slave functions • Programmable word clock, bit clock generation functions • Multichannel format functions (up to four channels) • Supports 8-/16-/18-/20-/22-/24-/32-bit data formats • Supports TDM mode • Supports WS continue mode • The DMA controller or interrupts control the transfer of data to and from the SSI module. • Supports short and long frames for monaural data (valid data lengths are 8 and 16 bits) • Up to nine independent clock signals can be input.
Audio clock generator (ADG)	• Selection or division of audio clock signals	

1.3.9 Storage

Item	Description
USB2.0 host & function module (USB2.0)	• 2 channels (Host only 1 channel/Host-Function 1 channel) • PHY integrated • USB Host (EHCI/OHCI) 2LINK • Compliance with USB2.0 • USB Function 1LINK • Compliance with USB2.0 (High-Speed) • Interrupt request • Internal dedicated DMA
SD host interface (SDHI)	• 3 channels — Interfaces 0: Support SDR104 class transfer rate at Max. 97.5 MBytes/sec. @ 195 MHz, and SDXC. Does not support CPRM. — Interfaces 1 and 2: Support SDR50 class transfer rate at Max. 48 MBytes/sec. @ 97.5 MHz, and SDXC. Does not support CPRM. • Supports SD memory/SDIO interface (1-/4-bit SD buses). • Error check function: CRC7 (command/response), CRC16 (data) • Card detection function • Supports write protection
Multi-media card interface (MMCIF)	• 1 channel • MMC 4.41 base • eMMC controllable • Data bus: 1/4/8-bit MMC mode (not support SPI mode) • Support block transfer (not support stream transfer) • Block size in multi-block transfer : 512 Bytes

1.3.10 Network

Item	Description
CAN interface (CAN)	• 2 channels • Supports CAN specification 2.0B • ISO-11898-1 compliant • Maximum bit rate: 1 Mbps • Message box — Normal mode: 32 receive-only mailboxes and 32 mailboxes for transmission/reception — FIFO mode: 32 receive-only mailboxes and 24 mailboxes for transmission/reception, 4-stage FIFO for transmission, and 4-stage FIFO for reception • Reception — Data frame and remote frame can be received. — Selectable receiving ID format — Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • Acceptance filter — Mask can be enabled or disabled for each mailbox. • Transmission — Data frame and remote frame can be transmitted. — Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) — Selectable ID priority mode or mailbox number priority mode • Sleep mode for reducing power consumption
Ethernet AVB	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Supports transfer at 1000 Mbps and 100 Mbps • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY GMII (Gigabit Media Independent Interface) and MII (Media Independent Interface)
Ethernet MAC	• IEEE802.3u MAC (Ether) function • Supports transfer at 10 and 100 Mbps • Flow control conforming to IEEE802.3x or back pressure system • Supports interface conforming to IEEE802.3u • Magic packet detection • Includes DMAC • Supports RMII (Reduced Media Independent Interface)

1.3.11 Timer

Item	Description
Watchdog timer (WDT)	• Single channel • Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time-period: more than 1 hour count capable
Timer pulse unit (TPU)	• 4-channels • 16-bit timers • Each channel outputs PWM

Item	Description
Compare match timer 0 (CMT0)	• Two channels • 32-bit timer (16 bits/32 bits can be selected) • Source clock: RCLK clock • Compare match function provided • Interrupt requests
Compare match timer 1 (CMT1)	• Eight channels • 48-bit timer (16 bits/32 bits/48 bits can be selected) • Source clock: RCLK/system clock • Compare match function provided • Interrupt requests
Timer unit (TMU)	• 4 sets of 3-channel 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request • 2 channels for input capture

1.3.12 Peripheral Module

Item	Description
I2C bus interface (IIC)	• 1 channel for 3.3 V LVTTL buffers and 1 channel for open drain type IO buffer • Supports single master transmission/reception • Interrupt request • DMAC request
Multi-master I2C bus interface (I2C)	• 6 channels for general purpose • Philips I2C bus interface method supported • Master/slave functions • Multi-master functions • Transfer rate up to 400 kbps supported • Programmable clock generation from the system clock
Serial communication interface with FIFO (SCIFA)	• 6 channels • Internal 64-Byte transmit/receive FIFOs • High-speed UART • Internal prescaler • Clock synchronous serial communications possible • Support edge selection function • Interrupt request, DMAC request and DMA multi-Byte transfer supported • Asynchronous mode • Clock synchronous mode
Serial communication interface with FIFO (SCIFB)	• 3 channels • Internal 256-Byte transmit/receive FIFOs • High-speed UART • Internal prescaler • Clock synchronous serial communications possible • Support edge selection function • Interrupt request, DMAC request and DMA multi-Byte transfer supported • Asynchronous mode (modem control is enabled) • Clock synchronous mode

Item	Description	
Serial communication interface with FIFO (SCIF)	Overall specification	• 6 channels • Asynchronous, clock-synchronized modes • Asynchronous serial communication mode The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats. — Data length: 7 bits or 8 bits — Stop bits: 1 bit or 2 bits — Parity: Even/odd/none — Receive error detection: Parity, framing, and overrun errors — Break detection: A break is detected when a framing error lasts for more than 1 frame length at Space 0 (low level). When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR). • Clock synchronous serial communication mode The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication. — Data length: 8 bits — Receive error detection: Overrun errors • Full-duplex communication capability The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception. • On-chip baud rate generator, enabling any bit rate to be selected The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock. • Eight interrupt sources The SCIF has eight types of interrupt sources: receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently. • DMA data transfer When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.

Item	Description
Clock-synchronized serial interface with FIFO (MSIOF)	• 3 channels • Max. speed: 26 Mbps • Internal 64-Byte transmit FIFOs/internal 256-Byte receive FIFOs • Supports master and slave modes • Internal prescaler • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request
Quad-SPI (QSPI)	• Single/Dual/Quad-SPI: serial slave transfer enabled • Supports master mode • SPCLK clock rate: 1…4080 in master mode; Max. 78 MHz
High-speed serial communication interface with FIFO (HSCIF)	• 3 channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS and HCTS) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.
PWM timer (PWM)	• 7 channels • High-level width (10 bits) of PWM output can be set. • High-level periods (10 bits) of PWM can be set. • Periods in the range from two to 2^{24} × 1024 cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable
Boot Function (BOOT)	• System startup with selectable boot mode at power-on reset • Program downloaded to internal memory (LRAM) • Autorun function for the downloaded program

1.3.13 Others

Item	Description
JTAG	JTAG interface for CoreSight
Process	28nm Si-CMOS
Package	FC-BGA2121-501

1.4 Power Supply Voltages and Temperature Range

- Power supply voltage (typ.)
  1.8 V: (ETM, SD, LVCMOS I/F, Xtal, JTAG, Trace and RST)
  1.03 V: (core)
  1.5 V: (DDR3-I/O SSTL Mode:DDR3)
  3.3 V: (Others)
- Temperature range
  Ta = –40°C to 85°C
  Tc = –40°C to 105°C

2. Area Map

See section 2, Area Map in the RZ/G Series User's Manual: Hardware.

3. Pin Assignment

3.1 Top View (Left)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSS	D12	D9	D4	D2	M0A12	M0A6	M0A10	M0A11	M0BA1	M0A2	M0A15	VSS
B	CLKOUT	EX_CS5#	D11	D6	D7	PRESET OUT#	M0A13	M0A5	M0A0	M0A3	M0A9	M0A1	M0A4
C	EX_CS4#	EX_WAIT0	VSS	D8	D5	D3	VDDQ_M0BK UP	VDDQ_M0	VSS	M0CK1#	M0CK1	VDDQ_M0	VSS
D	EX_CS2#	EX_CS3#	D14	VSS	D13	D0	M0A14	M0A8	M0ZQ	VSS	M0ODT1	M0RESET#	M0BA2
E	EX_CS0#	CS0#	EX_CS1#	D10	VSS	D1	M0BKPRST#	VDD_CPG PLL0	VSS_CPG PLL0	M0CS1#	M0CKE1	M0BA0	M0CAS#
F	A7/MD4	A5	A1/MD0	A0/MD3	D15	VSS	VSS	VSS	VSS	VSS	VSS	VDDQ_M0A PLL	VSSQ_M0A PLL
G	A13/MD6	A9/MD5	A12	A2/MDT1	A6	VCCQ18							
H	A15/MD7	A18/MDT0	A11	A4/MD1	A3/MD2	VCCQ18							
J	A24	A16	A23	A10	A8	VCCQ							
K	A21	A20	A19/MD18	A17	A14	VCCQ					VSS_CPG PLL3	VDD_CPG PLL3	VSS
L	WE0#/MD19	A25	A22	WE1#/MD20	DREQ0#	VSS				VSS	VSS_CPG PLL3	VDD_CPG PLL3	VSS
M	[RD/WR#] /MD9	DACK0 /MD21	RD#/MD14	BS#/MD8	CS1#/A26	VSS				VSS	VSS	VDD	VSS
N	VDD	VDD	VDD	VDD	VDD	VDD				VDD	VDD		
P	VDD	VDD	VDD	VDD	VDD	VDD				VSS	VSS	VDD	VSS
R	VCCQ	VCCQ	VCCQ	VCCQ	VCCQ	VCCQ				VSS	VSS	VDD	VSS
T	HSCIF0_ HSCK	HSCIF0_ HRTS#	HSCIF0_ HCTS#	HSCIF0_ HTX	ETH_MDIO	VSS				VSS	VSS	VDD	VSS
U	HSCIF0_HRX	ETH_TXD0	ETH_TX_EN	ETH_RXD1	ETH_RX_ER	VCCQ18							
V	ETH_REF_ CLK	ETH_TXD1	ETH_RXD0	ETH_CRS_ DV	ETH_LINK	VCCQ18							
W	VI0_VSYNC#	VI0_FIELD	VI0_DATA5 /VI0_B5	ETH_MAGIC	ETH_MDC	VSS							
Y	VI0_HSYNC#	VI0_DATA6 /VI0_B6	VI0_DATA4 /VI0_B4	I2C0_SDA	I2C0_SCL	VSS	VSS	VSS	VSS	VSS	VCCQ18	VCCQ18	VSS
AA	VI0_CLKENB	VI0_DATA7 /VI0_B7	VI0_DATA2 /VI0_B2	VI0_DATA0 /VI0_B0	VSS	SSI_SDATA0	SSI_WS0129	SD1_CMD	MMC_D0	MMC_D3	MMC_D1	SD0_DATA3	SD0_WP
AB	VI0_CLK	VI0_DATA3 /VI0_B3	VI0_DATA1 /VI0_B1	VSS	SSI_WS1	SSI_WS34	SSI_SDATA7	SD1_DATA2	MMC_D6	MMC_D4	MMC_D7	SD0_CD	DU0_CDE /MD13
AC	AUDIO_ CLKC	AUDIO_ CLKOUT	VSS	SSI_SDATA2	SSI_SDATA1	SSI_SDATA8	VCCQ_SD1	SD1_DATA3	MMC_D2	VCCQ_MMC _SD2	SD0_DATA0	VCCQ_SD0	DU0_EXODD F/DU0_ODD F/DISP/CDE
AD	AUDIO_ CLKA	SSI_SDATA9	SSI_WS9	SSI_WS2	SSI_SDATA3	SSI_SCK34	SD1_DATA0	SD1_CD	MMC_CMD	MMC_D5	SD0_DATA1	SD0_CMD	DU0_EXHSY NC/DU0_HS YNC/MD11
AE	VSS	AUDIO_ CLKB	SSI_SCK9	SSI_SCK2	SSI_SCK012 9	SSI_SCK1	SD1_DATA1	SD1_CLK	SD1_WP	MMC_CLK	SD0_DATA2	SD0_CLK	DU0_DOT CLKOUT1
	1	2	3	4	5	6	7	8	9	10	11	12	13

1/2 (left)

3.2 Top View (Right)

14	15	16	17	18	19	20	21	22	23	24	25	
M0CK0#	M0CK0	VSS	M0DQS1#	M0DQS1	VSS	M0DQS0#	M0DQS0	VSS	M0DQ6	M0DQ2	VSS	A
M0A7	VDDQ_M0	M0ODT0	M0DQ8	M0DQ14	M0DQ10	M0DQ11	VDDQ_M0	M0DQ3	M0DQ5	VSS	M0DQ22	B
M0VREFDQ0	M0CS0#	VSS	VDDQ_M0	VDDQ_M0	VSS	M0DQ4	M0DM0	M0DQ7	VSS	M0DQ23	M0DQ19	C
M0VREFCA	M0CKE0	M0RAS#	M0DQ9	M0DM1	M0DQ12	VSS	M0DQ1	VSS	VDDQ_M0	M0DQ21	VSS	D
M0WE#	VSSQ_M0D PLL1	VDDQ_M0D PLL1	VDDQ_M0	M0DQ15	M0DQ13	M0DQ0	VSS	M0DQ17	VSS	M0DQ18	M0DQS2#	E
VSS	VSSQ_M0D PLL0	VDDQ_M0D PLL0	VDDQ_M0	VSS	VSS	VSS	VSS	M0DM2	VDDQ_M0	M0DQ20	M0DQS2	F
						VSS	VSS	VSS	M0VREFDQ1	M0DQ16	VSS	G
						VSSQ_M0D PLL3	VSSQ_M0D PLL2	M0DQ26	VSS	VDDQ_M0	M0DQS3	H
						VDDQ_M0D PLL3	VDDQ_M0D PLL2	M0DM3	M0DQ24	M0DQ28	M0DQS3#	J
VDD	VDD_CPG PLL1	VSS_CPG PLL1				VDDQ_M0	VSS	M0DQ25	VSS	M0DQ30	VSS	K
VDD	VDD_CPG PLL1	VSS_CPG PLL1				VDDQ_M0	VSS	M0DQ27	VDDQ_M0	M0DQ29	M0DQ31	L
VDD	VSS	VSS				AVSS	VSS	VSS	VSS	USB1_RREF	USB0_RREF	M
	VDD	VDD				VSS	TRST#	TCK	VSS	USB1_DP	USB1_DM	N
VDD	VSS	VSS				VD331	TMS	TDO	AVDD	USB0_DP	USB0_DM	P
VDD	VSS	VSS				VD181	BSMODE	TDI	NMI	VSS	VSS	R
VDD	VSS	VSS				VCCQ18	USB1_PWEN	USB1_OVC	EXREFIN (VSS)	USB_XTAL	USB_EXTAL	T
						VCCQ18	USB0_PWEN	USB0_OVC	ACK	VSS	VSS	U
						VCCQ	VDD_MLB PLL	IIC1_SDA (I2C7)	PRESET#	XTAL	EXTAL	V
						VSS_MLB PLL	IIC1_SCL (I2C7)	MSIOF0_SS2	MSIOF0_ TXD	MSIOF0_ RXD	VSS	W
VSS	VCCQ	VCCQ	VSS	VSS	VSS	VSS	SSI_SDATA4	MSIOF0_SS1	HSCIF1_ HCTS#	I2C1_SCL	I2C1_SDA	Y
DU0_DB6	DU0_DB2	DU0_DG5	DU0_DG0	DU0_DR0	SSI_WS78	SSI_SDATA5	VSS	SCIF3_SCK	HSCIF1_ HTX	HSCIF1_ HSCK	MSIOF0_ SCK	AA
DU0_EXVSY NC/DU0_VS YNC/MD12	DU0_DB3	DU0_DG1	DU0_DG4	DU0_DR1	SSI_SCK78	SSI_WS5	SSI_WS4	VSS	HSCIF1_ HRX	HSCIF1_ HRTS#	MSIOF0_ SYNC	AB
DU0_DB0	DU0_DB7	DU0_DG7	DU0_DR6	DU0_DR3	DU0_DR7	I2C2_SDA	SCIF3_TXD	SCIF3_RXD	VSS	SCIF1_TXD	SCIF1_SCK	AC
DU0_DB4	DU0_DB5	DU0_DG3	DU0_DR5	DU0_DG2	DU0_DR4	SSI_WS6	I2C2_SCL	SSI_SCK4	SCIF2_RXD	MLB_REF	SCIF1_RXD	AD
DU0_DOTCL KOUT0	DU0_DOTCL KIN	DU0_DG6	DU0_DB1	DU0_DISP /MD10	DU0_DR2	SSI_SCK6	SSI_SDATA6	SSI_SCK5	SCIF2_TXD	SCIF2_SCK	VSS	AE
14	15	16	17	18	19	20	21	22	23	24	25	

2/2 (right)

: Multiplexed pin that function is selected by the Pin Function Controller (PFC) register and mode pin setting.

: Mode pin assigned.

3.3 Mode Pin Settings

Input fixed values for BSMODE pins. These values cannot be changed after power is supplied. The values of pins MD0 to MD14, MD18 to MD21, MDT0 and MDT1 are input upon power-on reset using the PRESET pin. Power-on reset results in switching to a different function.

Legend: "0" means logic low level input, "1" means logic high level input.
"—" means either "0" or "1", but its level must be fixed.

BSMODE	Reserved Fix to 0

MD0	Free-Running Mode or Step-Up Mode
0	Free-running mode
1	Step-up mode

MD3	MD2	MD1	Boot Device Selection
0	0	0	area 0 boot (boot from external MaskROM)
0	1	0	QSPI (48.75 MHz 16 KB transfer)
0	0	1	Reserved
0	1	1	Reserved
1	0	0	QSPI (39 MHz 16 KB transfer)
1	0	1	QSPI (78 MHz 16 KB transfer)
1	1	0	QSPI (39 MHz 4 KB transfer)
1	1	1	Reserved

MD4	Area Division
0	Area 0: 64 Mbytes
1	Area 0: 128 Mbytes

MD5	Reserved, fixed to 1

MD7	MD6	Master Boot Processor Selection
0	0	Setting prohibited
0	1	Cortex-A7 boot
1	0	Setting prohibited
1	1	Setting prohibited

MD8	EXBUS Area 0 Data Bus Width
0	8-bit
1	16-bit

MD9	EXTAL/XTAL Pin Setting
0	Inputs an external clock to the EXTAL pin
1	Connects a crystal resonator to the EXTAL/XTAL pin

MD12	MD10	MD21, MD20	MD11	MDT [1:0]	JTAG	SDHI1	MMC
0	0	00	—	—	Boundary SCAN	Normal mode	Normal mode
		01	—	—	Reserved	Reserved	Reserved
		10	0	—	Coresight debug port	Normal mode	Normal mode
			1	00		Reserved	Normal mode
				01		Reserved	Normal mode
				10		Normal mode	Reserved
				11		Normal mode	Reserved
		11	0	—	Reserved	Normal mode	Normal mode
			1	00		Coresight debug port	Normal mode
	1	00	—	—	Reserved	Reserved	Reserved
		01	0	—	Coresight debug port	Normal mode	Normal mode
			1	01		Reserved	Normal mode
		10	—	—	Reserved	Reserved	Reserved
		11	—	—	Reserved	Reserved	Reserved

MD14	MD13	Resonator/ Input Clock	Internal Divider	PLL1	PLL0	PLL3 /MD19: DDR3-1333
0	0	15 MHz	× 1/1	× 208*	× 200	× 88
0	1	20 MHz	× 1/1	× 156*	× 150	× 66
1	0	26 MHz	× 1/2	× 240*	× 230	× 102
1	1	30 MHz	× 1/2	× 208*	× 200	× 88

Note: * VCO = 3120 MHz

MD18	External Bus Clock
0	65 MHz (Fix to 0)
1	Setting Prohibited

MD19	DDR3-SDRAM Bus Clock
0	Setting Prohibited
1	DDR3-1333 mode (Fix to 1)

4. Pin Multiplexing

4.1 List of Multiplexed Pin Functions

Table 4.1 lists the multiplexed pin functions of the RZ/G1E.

The default pin function of each pin after power-on reset is "Function 1" respectively, unless otherwise mentioned.

For details on pin function control, refer to section 3.3, Mode Pin Settings and section 5, Pin Function Controller (PFC).

[Legend]

- Leftmost column of table
  No.: Serial number
  Pin No.: BGA package ball grid number
  Mode Pin (only for corresponding pin): Mode pin is assigned

- Middle column of table
  Function n (n=1, 2, 3, ...)/GPIO: Module or GPIO
  Module: Module abbreviation except for GPIO
  Pin Name: Module or GPIO pin name
  I/O: Input or output,
  i.e., I: Input, I(S): Schmitt input, IO: Input and output, IO (OD): Input and open drain output, O: Output, P: Power supply pin. (I)/(H)/(L)/(X)/(Z) with I, O or IO: Default pin state (only for default pin, except for clock or analog output), H: High level output, L: Low level output, X: Undefined value output, Z: High impedance

"Reserved" in module column is assigned optional function and "-" in module column is internal function or undefined, they must not be specified. This indication is different from that of in section 5, Pin Function Controller (PFC).

- Rightmost column of table
  During POR: Pin state during power-on reset (PRESET# pin input is low-level)
  V(power)/|IOH|: Pin voltage (power domain) and output drive current (nominal value respectively)
  Pull-up: Internal pull-up control function is available or not from a power-on reset
  "On": Pull-up control function is available and default state is pulled-up.
  (No.110, ACK pin is available for internal pull-down function.)
  "Off": Pull-up control function is available and default state is not pulled-up.
  "-": Pull-up control function is not available.
  For details of pull-up control function, refer to PUPR0 through PUPR6 registers in section 5, Pin Function Controller (PFC).

Notes: 1. Pin name that has an identifier for example "XXXX_B", "XXXX_C" etc. are mirror pins of the XXXX pin. Only one pin out of the XXXX pin or its mirror pins can be used. When using mirror pin, specify the suite of pin that has the same identifier for the selected module. It is prohibited to use a suite of pin as mixed two or more identifiers for a selected module.
2. Do not use any pins that of unused modules.
3. Unused pins must be handled as described in section 4.3, Handling of Unused Pins.
4. The terminal state after the reset cancellation has been described as a premise not using the BKPRST (BKRST#=H(fixed)).

Table 4.1 List of Multiplexed Pin Functions

DBSC3 (No.1 to 40): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
1	DBSC3	X
D15	M0CKE0	1.5/1.35V(VDDQ_M0BKUP)/-
	O(L)	-
2	DBSC3	X
E11	M0CKE1	1.5/1.35V(VDDQ_M0 BKUP)/-
	O(L)	-
3	DBSC3	P
D14	M0VREFCA	1.5/1.35V(VDDQ_M0 BKUP)/-
	P	-
4	DBSC3	I
E7	M0BKPRST#	1.5/1.35V(VDDQ_M0 BKUP)/-
	I	-
5	DBSC3	H
D12	M0RESET#	1.5/1.35V(VDDQ_M0BKUP)/-
	O(H to L)	-
6	DBSC3	X
A15	M0CK0	1.5/1.35V(VDDQ_M0)/-
	O	-
7	DBSC3	X
A14	M0CK0#	1.5/1.35V(VDDQ_M0)/-
	O	-
8	DBSC3	X
C11	M0CK1	1.5/1.35V(VDDQ_M0)/-
	O	-
9	DBSC3	X
C10	M0CK1#	1.5/1.35V(VDDQ_M0)/-
	O	-
10	DBSC3	H
C15	M0CS0#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
11	DBSC3	H
E10	M0CS1#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
12	DBSC3	L
B16	M0ODT0	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
13	DBSC3	L
D11	M0ODT1	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
14	DBSC3	IO
D9	M0ZQ	1.5/1.35V(VDDQ_M0)/-
	IO	-
15	DBSC3	H
E14	M0WE#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
16	DBSC3	H
D16	M0RAS#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
17	DBSC3	H
E13	M0CAS#	1.5/1.35V(VDDQ_M0)/-
	O(H)	-
18	DBSC3	L
B9	M0A0	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
19	DBSC3	L
B12	M0A1	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
20	DBSC3	L
A11	M0A2	1.5/1.35V(VDDQ_M0)/-
	O(L)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
21	DBSC3	L
B10	M0A3	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
22	DBSC3	L
B13	M0A4	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
23	DBSC3	L
B8	M0A5	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
24	DBSC3	L
A7	M0A6	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
25	DBSC3	L
B14	M0A7	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
26	DBSC3	L
D8	M0A8	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
27	DBSC3	L
B11	M0A9	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
28	DBSC3	L
A8	M0A10	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
29	DBSC3	L
A9	M0A11	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
30	DBSC3	L
A6	M0A12	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
31	DBSC3	L
B7	M0A13	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
32	DBSC3	L
D7	M0A14	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
33	DBSC3	L
A12	M0A15	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
34	DBSC3	L
E12	M0BA0	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
35	DBSC3	L
A10	M0BA1	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
36	DBSC3	L
D13	M0BA2	1.5/1.35V(VDDQ_M0)/-
	O(L)	-
37	DBSC3	P
F12	VDDQ_M0APLL	1.8V(VDDQ_M0APLL)/-
	P	-
38	DBSC3	P
F13	VSSQ_M0APLL	GND(VDDQ_M0APLL)/-
	P	-
39	DBSC3	Z
E20	M0DQ0	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
40	DBSC3	Z
D21	M0DQ1	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-

1/3 (DBSC3)

DBSC3 (No.41 to 80): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
41	DBSC3	Z
A24	M0DQ2	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
42	DBSC3	Z
B22	M0DQ3	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
43	DBSC3	Z
C20	M0DQ4	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
44	DBSC3	Z
B23	M0DQ5	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
45	DBSC3	Z
A23	M0DQ6	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
46	DBSC3	Z
C22	M0DQ7	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
47	DBSC3	Z*
A21	M0DQS0	1.5/1.35V(VDDQ_M0)/-
	IO(Z*)	-
48	DBSC3	Z*
A20	M0DQS0#	1.5/1.35V(VDDQ_M0)/-
	IO(Z*)	-
49	DBSC3	Z
C21	M0DM0	1.5/1.35V(VDDQ_M0)/-
	O(Z)	-
50	DBSC3	P
F16	VDDQ_M0DPLL0	1.8V(VDDQ_M0DPLL0)/-
	P	-
51	DBSC3	P
F15	VSSQ_M0DPLL0	GND(VDDQ_M0DPLL0)/-
	P	-
52	DBSC3	P
C14	M0VREFDQ0	1.5/1.35V(VDDQ_M0)/-
	P	-
53	DBSC3	Z
B17	M0DQ8	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
54	DBSC3	Z
D17	M0DQ9	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
55	DBSC3	Z
B19	M0DQ10	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
56	DBSC3	Z
B20	M0DQ11	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
57	DBSC3	Z
D19	M0DQ12	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
58	DBSC3	Z
E19	M0DQ13	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
59	DBSC3	Z
B18	M0DQ14	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
60	DBSC3	Z
E18	M0DQ15	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
61	DBSC3	Z*
A18	M0DQS1	1.5/1.35V(VDDQ_M0)/-
	IO(Z*)	-
62	DBSC3	Z*
A17	M0DQS1#	1.5/1.35V(VDDQ_M0)/-
	IO(Z*)	-
63	DBSC3	Z
D18	M0DM1	1.5/1.35V(VDDQ_M0)/-
	O(Z)	-
64	DBSC3	P
E16	VDDQ_M0DPLL1	1.8V(VDDQ_M0DPLL1)/-
	P	-
65	DBSC3	P
E15	VSSQ_M0DPLL1	GND(VDDQ_M0DPLL1)/-
	P	-
66	DBSC3	Z
G24	M0DQ16	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
67	DBSC3	Z
E22	M0DQ17	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
68	DBSC3	Z
E24	M0DQ18	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
69	DBSC3	Z
C25	M0DQ19	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
70	DBSC3	Z
F24	M0DQ20	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
71	DBSC3	Z
D24	M0DQ21	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
72	DBSC3	Z
B25	M0DQ22	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
73	DBSC3	Z
C24	M0DQ23	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
74	DBSC3	Z*
F25	M0DQS2	1.5/1.35V(VDDQ_M0)/-
	IO(Z*)	-
75	DBSC3	Z*
E25	M0DQS2#	1.5/1.35V(VDDQ_M0)/-
	IO(Z*)	-
76	DBSC3	Z
F22	M0DM2	1.5/1.35V(VDDQ_M0)/-
	O(Z)	-
77	DBSC3	P
J21	VDDQ_M0DPLL2	-
	P	-
78	DBSC3	P
H21	VSSQ_M0DPLL2	GND(VDDQ_M0DPLL2)/-
	P	-
79	DBSC3	P
G23	M0VREFDQ1	1.5/1.35V(VDDQ_M0)/-
	P	-
80	DBSC3	Z
J23	M0DQ24	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-

2/3 (DBSC3)

Note: No.47, 48, 61, 62, 74 and 75 (M0DQSx and M0DQSx#) pin states during POR and default state:
The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the MnDQSx pin and high-level for the MnDQSx# pin respectively.

DBSC3 (No.81 to 93): Single Function

	Function 1	
No.	**Module**	**During POR**
Pin No.	**Pin Name**	**V(power)/|IOH|**
	I/O	**Pull-up**
81	DBSC3	Z
K22	M0DQ25	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
82	DBSC3	Z
H22	M0DQ26	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
83	DBSC3	Z
L22	M0DQ27	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
84	DBSC3	Z
J24	M0DQ28	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
85	DBSC3	Z
L24	M0DQ29	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
86	DBSC3	Z
K24	M0DQ30	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
87	DBSC3	Z
L25	M0DQ31	1.5/1.35V(VDDQ_M0)/-
	IO(Z)	-
88	DBSC3	Z*
H25	M0DQS3	1.5/1.35V(VDDQ_M0)/-
	IO(Z*)	-
89	DBSC3	Z*
J25	M0DQS3#	1.5/1.35V(VDDQ_M0)/-
	IO(Z*)	-
90	DBSC3	Z
J22	M0DM3	1.5/1.35V(VDDQ_M0)/-
	O(Z)	-
91	DBSC3	P
J20	VDDQ_M0DPLL3	1.8V(VDDQ_M0DPLL3)/-
	P	-
92	DBSC3	P
H20	VSSQ_M0DPLL3	GND(VDDQ_M0DPLL3)/-
	P	-
93	DBSC3	P
C7	VDDQ_M0BKUP	1.5/1.35V(VDDQ_M0BKUP)/-
	P	-

3/3 (DBSC3)

Note: No.88 and 89 (M0DQS3 and M0DQS3#) pin states during POR and default state:
The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQS3 pin and high-level for the M0DQS3# pin respectively.

CPG, RESET, SYSTEM, Debug, USB (No.94 to 116): Single Function

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
94	CPG	I
V25	EXTAL	1.8V(VCCQ18)/-
	I	-
95	CPG	O
V24	XTAL	1.8V(VCCQ18)/-
	O	-
96	PLL	P
E8	VDD_CPGPLL0	1.8V(VDD_CPGPLL0)/-
	P	-
97	PLL	P
E9	VSS_CPGPLL0	GND(VDD_CPGPLL0)/-
	P	-
98	PLL	P
K15/L15	VDD_CPGPLL1	1.8V(VDD_CPGPLL1)/-
	P	-
99	PLL	P
K16/L16	VSS_CPGPLL1	GND(VDD_CPGPLL1)/-
	P	-
100	PLL	P
K12/L12	VDD_CPGPLL3	1.8V(VDD_CPGPLL3)/-
	P	-
101	PLL	P
K11/L11	VSS_CPGPLL3	GND(VDD_CPGPLL3)/-
	P	-
102	RESET	I(S, L)
V23	PRESET#	1.8V(VCCQ18)/-
	I(S)	-
103	RESET	O(L)
B6	PRESETOUT#	3.3V(VCCQ18)/4mA
	O(L to H)	-
104	SYSTEM	I(S)
R21	BSMODE	1.8V(VCCQ18)/-
	I(S)	-
105	Debug	I
N21	TRST#	1.8V(VCCQ18)/-
	I	On

	Function 1	
No.	Module	During POR
Pin No.	Pin Name	V(power)/|IOH|
	I/O	Pull-up
106	Debug	I
N22	TCK	1.8V(VCCQ18)/-
	I	On
107	Debug	I
P21	TMS	1.8V(VCCQ18)/-
	I	On
108	Debug	I
R22	TDI	1.8V(VCCQ18)/-
	I	On
109	Debug	Z
P22	TDO	1.8V(VCCQ18)/4mA
	O(Z)	-
110	Debug	I
U23	ACK	1.8V(VCCQ18)/4mA
	IO(I)	On(pull-down)
111	USB	I
T25	USB_EXTAL	1.8V(VCCQ18)/-
	I	-
112	USB	O
T24	USB_XTAL	1.8V(VCCQ18)/-
	O	-
113	USB	P
P20	VD331	3.3V(VD331)/-
	P	-
114	USB	P
R20	VD181	1.8V(VD181)/-
	P	-
115	USB	P
P23	AVDD	1.8V(AVDD)/-
	P	-
116	USB	P
M20	AVSS	GND(AVDD)/-
	P	-

USB 2.0, INTC, SDHI and GPIO (No.117 to 136): Up to 2-Function Multiplexed

Following pins multiplexed with the GPIO are set for GPIO function after power-on reset except for USB pins. For details, refer to GPSR5 and GPSR6 registers in section 5, Pin Function Controller (PFC).

	Function 1	GPIO	
No.	Module		During POR
Pin No.	Pin Name		V(power)/|IOH|
	I/O		Pull-up
117	USB 2.0 ch0	-	I
P24	USB0_DP	-	3.3V(VD331)/-
	IO(I)	-	-
118	USB 2.0 ch0	-	I
P25	USB0_DM	-	3.3V(VD331)/-
	IO(I)	-	-
119	USB 2.0 ch0	-	I
M25	USB0_RREF	-	3.3V(VCCQ)/-
	I	-	-
120	USB 2.0 ch0		Z(USB)
U21	USB0_PWEN	GP5_24	3.3V(VCCQ)/4mA
	O(L)	IO	-
121	USB 2.0 ch0		I(USB)
U22	USB0_OVC	GP5_25	3.3V(VCCQ)/4mA
	I(I)	IO	On
122	USB 2.0 ch1	-	I
N24	USB1_DP	-	3.3V(VCCQ)/-
	IO(I)	-	-
123	USB 2.0 ch1	-	I
N25	USB1_DM	-	3.3V(VCCQ)/-
	IO(I)	-	-
124	USB 2.0 ch1	-	I
M24	USB1_RREF	-	3.3V(VCCQ)/-
	I	-	-
125	USB 2.0 ch1		Z(USB)
T21	USB1_PWEN	GP5_26	3.3V(VCCQ)/4mA
	O(L)	IO	-
126	USB 2.0 ch1		I(USB)
T22	USB1_OVC	GP5_27	3.3V(VCCQ)/4mA
	I(I)	IO	-
127	INTC	-	I(S)
R23	NMI	-	1.8V(VCCQ18)/-
	I(S)	-	-
128	SDHI0		I(GPIO)
AE12	SD0_CLK	GP6_0	1.8/3.3V(VCCQ_SD0)/16mA
	O	IO(I)	-
129	SDHI0		I(GPIO)
AD12	SD0_CMD	GP6_1	1.8/3.3V(VCCQ_SD0)/16mA
	IO	IO(I)	Off
130	SDHI0		I(GPIO)
AC11	SD0_DATA0	GP6_2	1.8/3.3V(VCCQ_SD0)/16mA
	IO	IO(I)	Off
131	SDHI0		I(GPIO)
AD11	SD0_DATA1	GP6_3	1.8/3.3V(VCCQ_SD0)/16mA
	IO	IO(I)	Off
132	SDHI0		I(GPIO)
AE11	SD0_DATA2	GP6_4	1.8/3.3V(VCCQ_SD0)/16mA
	IO	IO(I)	Off
133	SDHI0		I(GPIO)
AA12	SD0_DATA3	GP6_5	1.8/3.3V(VCCQ_SD0)/16mA
	IO	IO(I)	Off
134	SDHI0		I(GPIO)
AB12	SD0_CD	GP6_6	1.8/3.3V(VCCQ_SD0)/16mA
	I	IO(I)	Off
135	SDHI0		I(GPIO)
AA13	SD0_WP	GP6_7	1.8/3.3V(VCCQ_SD0)/16mA
	I	IO(I)	Off
136	SDHI0 Power	-	P
AC12	VCCQ_SD0	-	1.8/3.3V(VCCQ_SD0)/-
	P	-	-

Note: (No.128 to 135): Pin voltage is selectable (3.3 V: default). For details, refer to IOCTRL3 register in section 5, Pin Function Controller (PFC).

SDHI, INTC, RCAN, MMC, SCIF, I2C and GPIO (No.137 to 156): Up to 5-Function Multiplexed

Pin states during POR and default pin function (GPIO or DBG: debugging mode) after power-on reset depend on mode pins setting except for No.145 and 156. For details, refer to Mode Pin Settings in section 3.3, GPSR6 register in section 5, Pin Function Controller (PFC) and section 62, CoreSight for DBG.

Function	1	2	3	4	GPIO	
No.	Module	-				During POR
Pin No.	Pin Name	-				V(power)/|IOH|
	I/O	-				Pull-up
137	SDHI1	-	-	-		I(GPIO)/Z(DBG)
AE8	SD1_CLK	-	-	-	GP6_8	1.8/3.3V(VCCQ_SD1)*/16mA
	O	-	-	-	IO(I)	-
138	SDHI1	-	-	-		I(GPIO)/I(DBG)
AA8	SD1_CMD	-	-	-	GP6_9	1.8/3.3V(VCCQ_SD1)*/16mA
	IO	-	-	-	IO(I)	Off
139	SDHI1	-	-	-		I(GPIO)/I(DBG)
AD7	SD1_DATA0	-	-	-	GP6_10	1.8/3.3V(VCCQ_SD1)*/16mA
	IO	-	-	-	IO(I)	Off
140	SDHI1	-	-	-		I(GPIO)/I(DBG)
AE7	SD1_DATA1	-	-	-	GP6_11	1.8/3.3V(VCCQ_SD1)*/16mA
	IO	-	-	-	IO(I)	Off
141	SDHI1	-	-	-		I(GPIO)/I(DBG)
AB8	SD1_DATA2	-	-	-	GP6_12	1.8/3.3V(VCCQ_SD1)*/16mA
	IO	-	-	-	IO(I)	Off
142	SDHI1	-	-	-		I(GPIO)/I(DBG)
AC8	SD1_DATA3	-	-	-	GP6_13	1.8/3.3V(VCCQ_SD1)*/16mA
	IO	-	-	-	IO(I)	Off
143	SDHI1	RCAN0	-	-		I(GPIO)
AD8	SD1_CD	CAN0_RX	-	-	GP6_14	1.8/3.3V(VCCQ_SD1)*/16mA
	I	I	-	-	IO(I)	Off
144	SDHI1	INTC	RCAN0	-		I(GPIO)
AE9	SD1_WP	IRQ7	CAN0_TX	-	GP6_15	1.8/3.3V(VCCQ_SD1)*/16mA
	I	I	O	-	IO(I)	Off
145	SDHI1Power	-	-	-	-	P
AC7	VCCQ_SD1	-	-	-	-	1.8/3.3V(VCCQ_SD1)/-
	P	-	-	-	-	-
146	MMC	SDHI2	-	-		I(GPIO)/Z(DBG)
AE10	MMC_CLK	SD2_CLK	-	-	GP6_16	1.8/3.3V(VCCQ_MMC_SD2)*/16mA
	O	O	-	-	IO(I)	-
147	MMC	SDHI2	-	-		I(GPIO)/I(DBG)
AD9	MMC_CMD	SD2_CMD	-	-	GP6_17	1.8/3.3V(VCCQ_MMC_SD2)*/16mA
	IO	IO	-	-	IO(I)	Off
148	MMC	SDHI2	-	-		I(GPIO)/I(DBG)
AA9	MMC_D0	SD2_DATA0	-	-	GP6_18	1.8/3.3V(VCCQ_MMC_SD2)*/16mA
	IO	IO	-	-	IO(I)	Off
149	MMC	SDHI2	-	-		I(GPIO)/I(DBG)
AA11	MMC_D1	SD2_DATA1	-	-	GP6_19	1.8/3.3V(VCCQ_MMC_SD2)*/16mA
	IO	IO	-	-	IO(I)	Off
150	MMC	SDHI2	-	-		I(GPIO)/I(DBG)
AC9	MMC_D2	SD2_DATA2	-	-	GP6_20	1.8/3.3V(VCCQ_MMC_SD2)*/16mA
	IO	IO	-	-	IO(I)	Off
151	MMC	SDHI2	-	-		I(GPIO)/I(DBG)
AA10	MMC_D3	SD2_DATA3	-	-	GP6_21	1.8/3.3V(VCCQ_MMC_SD2)*/16mA
	IO	IO	-	-	IO(I)	Off
152	MMC	SDHI2	-	-		I(GPIO)
AB10	MMC_D4	SD2_CD	-	-	GP6_22	1.8/3.3V(VCCQ_MMC_SD2)*/16mA
	IO	I	-	-	IO(I)	Off
153	MMC	SDHI2	-	-		I(GPIO)
AD10	MMC_D5	SD2_WP	-	-	GP6_23	1.8/3.3V(VCCQ_MMC_SD2)*/16mA
	IO	I	-	-	IO(I)	Off
154	MMC	SCIF0	I2C2	RCAN1		I(GPIO)
AB9	MMC_D6	SCIF0_RXD	I2C2_SCL_B	CAN1_RX	GP6_24	3.3V(VCCQ)/16mA
	IO	I	IO	I	IO(I)	Off
155	MMC	SCIF0	I2C2	RCAN1		I(GPIO)
AB11	MMC_D7	SCIF0_TXD	I2C2_SDA_B	CAN1_TX	GP6_25	3.3V(VCCQ)/16mA
	IO	O	IO	O	IO(I)	Off
156	MMC_SDHI2 Power	-	-	-	-	P
AC10	VCCQ_MMC_SD2	-	-	-	-	1.8/3.3V(VCCQ_MMC_SD2)/-
	P	-	-	-	-	-

Note: (No.137 to 144 and 146 to 155): Pin voltage is selectable (3.3 V: default) for each SDHI channel and multiplexed GPIO pins suite. For details, refer to IOCTRL3 register in section 5, Pin Function Controller (PFC).

LBSC, SCIFA, INTC, I2C, SCIF, TMU, PWM, HSCIF, SCIFB and GPIO (No.157 to 176): Up to 6-Function Multiplexed and Mode Pin assigned (No.173 to 176)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting.

When MD[3:1]=000, the LBSC will execute area 0 booting.

Function	1	2	3	4	5	GPIO	
MD[3:1]	=000					≠000	
No.							During POR
Pin No.							V(power)/|IOH|
Mode Pin							Pull-up
157	LBSC	SCIFA3	INTC	-	-		I(GPIO)
D6	D0	SCIFA3_SCK_B	IRQ4	-	-	GP0_0	3.3V(VCCQ)/8mA
	IO(I)	O	I	-	-	IO(I)	On
158	LBSC	SCIFA3	-	-	-		I(GPIO)
E6	D1	SCIFA3_RXD_B	-	-	-	GP0_1	3.3V(VCCQ)/8mA
	IO(I)	I	-	-	-	IO(I)	On
159	LBSC	SCIFA3	-	-	-		I(GPIO)
A5	D2	SCIFA3_TXD_B	-	-	-	GP0_2	3.3V(VCCQ)/8mA
	IO(I)	O	-	-	-	IO(I)	On
160	LBSC	I2C3	SCIF5	-	-		I(GPIO)
C6	D3	I2C3_SCL_B	SCIF5_RXD_B	-	-	GP0_3	3.3V(VCCQ)/8mA
	IO(I)	IO	I	-	-	IO(I)	On
161	LBSC	I2C3	SCIF5	-	-		I(GPIO)
A4	D4	I2C3_SDA_B	SCIF5_TXD_B	-	-	GP0_4	3.3V(VCCQ)/8mA
	IO(I)	IO	O	-	-	IO(I)	On
162	LBSC	SCIF4	I2C0	-	-		I(GPIO)
C5	D5	SCIF4_RXD_B	I2C0_SCL_D	-	-	GP0_5	3.3V(VCCQ)/8mA
	IO(I)	I	IO	-	-	IO(I)	On
163	LBSC	SCIF4	I2C0	-	-		I(GPIO)
B4	D6	SCIF4_TXD_B	I2C0_SDA_D	-	-	GP0_6	3.3V(VCCQ)/8mA
	IO(I)	O	IO	-	-	IO(I)	On
164	LBSC	INTC	TMU	PWM6	-		I(GPIO)
B5	D7	IRQ3	TCLK1	PWM6_B	-	GP0_7	3.3V(VCCQ)/8mA
	IO(I)	I	I	O	-	IO(I)	On
165	LBSC	HSCIF2	I2C1	-	-		I(GPIO)
C4	D8	HSCIF2_HRX	I2C1_SCL_B	-	-	GP0_8	3.3V(VCCQ)/8mA
	IO(I)	I	IO	-	-	IO(I)	On
166	LBSC	HSCIF2	I2C1	-	-		I(GPIO)
A3	D9	HSCIF2_HTX	I2C1_SDA_B	-	-	GP0_9	3.3V(VCCQ)/8mA
	IO(I)	O	IO	-	-	IO(I)	On
167	LBSC	HSCIF2	SCIF1	INTC	PWM5		I(GPIO)
E4	D10	HSCIF2_HSCK	SCIF1_SCK_C	IRQ6	PWM5_C	GP0_10	3.3V(VCCQ)/8mA
	IO(I)	IO	IO	I	O	IO(I)	On
168	LBSC	HSCIF2	SCIF1	I2C1	-		I(GPIO)
B3	D11	HSCIF2_HCTS#	SCIF1_RXD_C	I2C1_SCL_D	-	GP0_11	3.3V(VCCQ)/8mA
	IO(I)	IO	I	IO	-	IO(I)	On
169	LBSC	HSCIF2	SCIF1	I2C1	-		I(GPIO)
A2	D12	HSCIF2_HRTS#	SCIF1_TXD_C	I2C1_SDA_D	-	GP0_12	3.3V(VCCQ)/8mA
	IO(I)	IO	O	IO	-	IO(I)	On
170	LBSC	SCIFA1	Reserved	PWM2	TMU		I(GPIO)
D5	D13	SCIFA1_SCK	-	PWM2_C	TCLK2_B	GP0_13	3.3V(VCCQ)/8mA
	IO(I)	O	-	O	I	IO(I)	On
171	LBSC	SCIFA1	I2C5	-	-		I(GPIO)
D3	D14	SCIFA1_RXD	I2C5_SCL_B	-	-	GP0_14	3.3V(VCCQ)/8mA
	IO(I)	I	IO	-	-	IO(I)	On
172	LBSC	SCIFA1	I2C5	-	-		I(GPIO)
F5	D15	SCIFA1_TXD	I2C5_SDA_B	-	-	GP0_15	3.3V(VCCQ)/8mA
	IO(I)	O	IO	-	-	IO(I)	On
173	LBSC	SCIFB1	PWM3	-	-		I(Mode Pin)
F4	A0	SCIFB1_SCK	PWM3_B	-	-	GP0_16	3.3V(VCCQ)/8mA
MD3	O(L)	O	O	-	-	IO(I)	Off
174	LBSC	SCIFB1	-	-	-		I(Mode Pin)
F3	A1	SCIFB1_TXD	-	-	-	GP0_17	3.3V(VCCQ)/8mA
MD0	O(L)	O	-	-	-	IO(I)	Off
175	LBSC	-	-	-	-		I(Mode Pin)
G4	A2	-	-	-	-	GP0_18	3.3V(VCCQ)/8mA
MDT1	O(L)	-	-	-	-	IO(I)	Off
176	LBSC	SCIFB0	-	-	-		I(Mode Pin)
H5	A3	SCIFB0_SCK	-	-	-	GP0_19	3.3V(VCCQ)/8mA
MD2	O(L)	O	-	-	-	IO(I)	Off

LBSC, SCIFB, PWM, TPU, SCIFA, MSIOF, IIC, HSCIF, RCAN, QSPI and GPIO (No.177 to 196): Up to 8-Function Multiplexed and Mode Pin assigned (No.177, 180, 182, 186, 188, 191 and 192)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting.
When MD[3:1]=000, the LBSC will execute area 0 booting; MD[3:1]≠000, the QSPI will execute QSPI booting.

Function	1	2	3	4	5	6	7	GPIO	
MD[3:1]	=000							≠000	
No.									During POR
Pin No.									V(power)/|IOH|
Mode Pin									Pull-up
177	LBSC	SCIFB0	-	-	-	-	-		I(Mode Pin)
H4	A4	SCIFB0_TXD	-	-	-	-	-	GP0_20	3.3V(VCCQ)/8mA
MD1	O(L)	O	-	-	-	-	-	IO(I)	Off
178	LBSC	SCIFB0	PWM4	TPU	-	-	-		I(GPIO)
F2	A5	SCIFB0_RXD	PWM4_B	TPUTO3_C	-	-	-	GP0_21	3.3V(VCCQ)/8mA
	O(L)	I	O	O	-	-	-	IO(I)	On
179	LBSC	SCIFB0	SCIFA4	TPU	-	-	-		I(GPIO)
G5	A6	SCIFB0_CTS#	SCIFA4_RXD_B	TPUTO2_C	-	-	-	GP0_22	3.3V(VCCQ)/8mA
	O(L)	I	I	O	-	-	-	IO(I)	On
180	LBSC	SCIFB0	SCIFA4	-	-	-	-		I(Mode Pin)
F1	A7	SCIFB0_RTS#	SCIFA4_TXD_B	-	-	-	-	GP0_23	3.3V(VCCQ)/8mA
MD4	O(L)	O	O	-	-	-	-	IO(I)	Off
181	LBSC	MSIOF1	SCIFA0	-	-	-	-		I(GPIO)
J5	A8	MSIOF1_RXD	SCIFA0_RXD_B	-	-	-	-	GP0_24	3.3V(VCCQ)/8mA
	O(L)	I	I	-	-	-	-	IO(I)	On
182	LBSC	MSIOF1	SCIFA0	-	-	-	-		I(Mode Pin)
G2	A9	MSIOF1_TXD	SCIFA0_TXD_B	-	-	-	-	GP0_25	3.3V(VCCQ)/8mA
MD5	O(L)	O	O	-	-	-	-	IO(I)	Off
183	LBSC	MSIOF1	IIC0(I2C6)	-	-	-	-		I(GPIO)
J4	A10	MSIOF1_SCK	IIC0_SCL_B	-	-	-	-	GP0_26	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	-	-	IO(I)	On
184	LBSC	MSIOF1	IIC0(I2C6)	-	-	-	-		I(GPIO)
H3	A11	MSIOF1_SYNC	IIC0_SDA_B	-	-	-	-	GP0_27	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	-	-	IO(I)	On
185	LBSC	MSIOF1	SCIFA5	-	-	-	-		I(GPIO)
G3	A12	MSIOF1_SS1	SCIFA5_RXD_B	-	-	-	-	GP0_28	3.3V(VCCQ)/8mA
	O(L)	O	I	-	-	-	-	IO(I)	On
186	LBSC	MSIOF1	SCIFA5	-	-	-	-		I(Mode Pin)
G1	A13	MSIOF1_SS2	SCIFA5_TXD_B	-	-	-	-	GP0_29	3.3V(VCCQ)/8mA
MD6	O(L)	O	O	-	-	-	-	IO(I)	Off
187	LBSC	MSIOF2	HSCIF0	LBSC	-	-	-		I(GPIO)
K5	A14	MSIOF2_RXD	HSCIF0_HRX_B	DREQ1#	-	-	-	GP0_30	3.3V(VCCQ)/8mA
	O(L)	I	I	I	-	-	-	IO(I)	On
188	LBSC	MSIOF2	HSCIF0	LBSC	-	-	-		I(Mode Pin)
H1	A15	MSIOF2_TXD	HSCIF0_HTX_B	DACK1	-	-	-	GP0_31	3.3V(VCCQ)/8mA
MD7	O(L)	O	O	O	-	-	-	IO(I)	Off
189	LBSC	MSIOF2	HSCIF0	Reserved	Reserved	RCAN	TPU		I(GPIO)
J2	A16	MSIOF2_SCK	HSCIF0_HSCK_B	-	-	CAN_CLK_C	TPUTO2_B	GP1_0	3.3V(VCCQ)/8mA
	O(L)	IO	IO	-	-	I	O	IO(I)	On
190	LBSC	MSIOF2	SCIF4	RCAN1	-	-	-		I(GPIO)
K4	A17	MSIOF2_SYNC	SCIF4_RXD_E	CAN1_RX_B	-	-	-	GP1_1	3.3V(VCCQ)/8mA
	O(L)	IO	I	I	-	-	-	IO(I)	On
191	LBSC	MSIOF2	SCIF4	RCAN1	-	-	-		I(Mode Pin)
H2	A18	MSIOF2_SS1	SCIF4_TXD_E	CAN1_TX_B	-	-	-	GP1_2	3.3V(VCCQ)/8mA
MDT0	O(L)	O	O	O	-	-	-	IO(I)	Off
192	LBSC	MSIOF2	PWM4	TPU	Reserved	-	-		I(Mode Pin)
K3	A19	MSIOF2_SS2	PWM4	TPUTO2	-	-	-	GP1_3	3.3V(VCCQ)/8mA
MD18	O(L)	O	O	O	-	-	-	IO(I)	Off
193	LBSC	QSPI	Reserved	-	-	-	-		I(GPIO)
K2	A20	SPCLK	-	-	-	-	-	GP1_4	3.3V(VCCQ)/8mA
	O(L)	IO	-	-	-	-	-	IO(I)	On
194	LBSC	QSPI	Reserved	-	-	-	-		I(GPIO)
K1	A21	MOSI/IO0	-	-	-	-	-	GP1_5	3.3V(VCCQ)/8mA
	O(L)	IO	-	-	-	-	-	IO(I)	On
195	LBSC	QSPI	Reserved	LBSC	-	-	-		I(GPIO)
L3	A22	MISO/IO1	-	ATADIR1#	-	-	-	GP1_6	3.3V(VCCQ)/8mA
	O(L)	IO	-	O	-	-	-	IO(I)	On
196	LBSC	QSPI	Reserved	LBSC	-	-	-		I(GPIO)
J3	A23	IO2	-	ATAWR1#	-	-	-	GP1_7	3.3V(VCCQ)/8mA
	O(L)	IO	-	O	-	-	-	IO(I)	On

LBSC, QSPI, VIN, TPU, SCIFB, PWM, SCIF, SCIFA, I2C, RCAN and GPIO (No.197 to 215): Up to 9-Function Multiplexed and Mode Pin assigned (No.208 to 212 and 215)

Default pin function (function 1 or GPIO) after power-on reset is defined by MD[3:1] pins setting except for No.199, 202 to 207, 210, 214 and 215.
When MD[3:1]=000, the LBSC will execute area 0 booting; MD[3:1]≠000, the QSPI will execute QSPI booting.

Function	1	2	3	4	5	6	7	8	GPIO	
MD[3:1]	=000								≠000	
No.										During POR
Pin No.										V(power)/|IOH|
Mode Pin										Pull-up
197	LBSC	QSPI	LBSC	-	-	-	-	-		I(GPIO)
J1	A24	IO3	EX_WAIT2	-	-	-	-	-	GP1_8	3.3V(VCCQ)/8mA
	O(L)	IO	I	-	-	-	-	-	IO(I)	On
198	LBSC	QSPI	LBSC	-	-	-	-	-		I(GPIO)
L2	A25	SSL	ATARD1#	-	-	-	-	-	GP1_9	3.3V(VCCQ)/8mA
	O(L)	IO	O	-	-	-	-	-	IO(I)	On
199	LBSC	-	-	-	-	-	-	-	-	O
B1	CLKOUT	-	-	-	-	-	-	-	-	3.3V(VCCQ)/8mA
	O	-	-	-	-	-	-	-	-	-
200	LBSC	VIN1	-	-	-	-	-	-		I(GPIO)
E2	CS0#	VI1_DATA8	-	-	-	-	-	-	GP1_10	3.3V(VCCQ)/4mA
	O(H)	I	-	-	-	-	-	-	IO(I)	On
201	LBSC	VIN1	-	-	-	-	-	-		I(GPIO)
M5	CS1#/A26	VI1_DATA9	-	-	-	-	-	-	GP1_11	3.3V(VCCQ)/4mA
	O(H/L)*	I	-	-	-	-	-	-	IO(I)	On
202	LBSC	VIN1	-	-	-	-	-	-		I(GPIO)
E1	EX_CS0#	VI1_DATA10	-	-	-	-	-	-	GP1_12	3.3V(VCCQ)/4mA
	O	I	-	-	-	-	-	-	IO(I)	On
203	LBSC	TPU	SCIFB2	VIN1	-	-	-	-		I(GPIO)
E3	EX_CS1#	TPUTO3_B	SCIFB2_RXD	VI1_DATA11	-	-	-	-	GP1_13	3.3V(VCCQ)/4mA
	O	O	I	I	-	-	-	-	IO(I)	On
204	LBSC	PWM0	SCIF4	Reserved	Reserved	TPU	SCIFB2	Reserved		I(GPIO)
D1	EX_CS2#	PWM0	SCIF4_RXD_C	-	-	TPUTO3	SCIFB2_TXD	-	GP1_14	3.3V(VCCQ)/4mA
	O	O	I	-	-	O	O	-	IO(I)	On
205	LBSC	SCIFA2	SCIF4	Reserved	Reserved	Reserved	SCIFB2	Reserved		I(GPIO)
D2	EX_CS3#	SCIFA2_SCK	SCIF4_TXD_C	-	-	-	SCIFB2_SCK	-	GP1_15	3.3V(VCCQ)/8mA
	O	O	O	-	-	-	O	-	IO(I)	On
206	LBSC	SCIFA2	I2C2	Reserved	Reserved	Reserved	SCIFB2	Reserved		I(GPIO)
C1	EX_CS4#	SCIFA2_RXD	I2C2_SCL_E	-	-	-	SCIFB2_CTS#	-	GP1_16	3.3V(VCCQ)/4mA
	O	I	IO	-	-	-	I	-	IO(I)	On
207	LBSC	SCIFA2	I2C2	Reserved	Reserved	Reserved	SCIFB2	Reserved		I(GPIO)
B2	EX_CS5#	SCIFA2_TXD	I2C2_SDA_E	-	-	-	SCIFB2_RTS#	-	GP1_17	3.3V(VCCQ)/4mA
	O	O	IO	-	-	-	O	-	IO(I)	On
208	LBSC	LBSC	PWM1	TPU	LBSC	Reserved	-	-		I(Mode Pin)
M4	BS#	DRACK0	PWM1_C	TPUTO0_C	ATACS01#	-	-	-	GP1_18	3.3V(VCCQ)/4mA
MD8	O(H)	O	O	O	O	-	-	-	IO(I)	Off
209	LBSC	LBSC	-	-	-	-	-	-		I(Mode Pin)
M3	RD#	ATACS11#	-	-	-	-	-	-	GP1_19	3.3V(VCCQ)/4mA
MD14	O(H)	O	-	-	-	-	-	-	IO(I)	Off
210	LBSC	LBSC	-	-	-	-	-	-		I(Mode Pin)
M1	RD/WR#	ATAG1#	-	-	-	-	-	-	GP1_20	3.3V(VCCQ)/4mA
MD9	O	O	-	-	-	-	-	-	IO(I)	Off
211	LBSC	-	-	-	-	-	-	-		I(Mode Pin)
L1	WE0#	-	-	-	-	-	-	-	GP1_21	3.3V(VCCQ)/4mA
MD19	O(H)	-	-	-	-	-	-	-	IO(I)	Off
212	LBSC	-	-	-	-	-	-	-		I(Mode Pin)
L4	WE1#	-	-	-	-	-	-	-	GP1_22	3.3V(VCCQ)/4mA
MD20	O(H)	-	-	-	-	-	-	-	IO(I)	Off
213	LBSC	RCAN	SCIF	Reserved	-	-	-	-		I(GPIO)
C2	EX_WAIT0	CAN_CLK_B	SCIF_CLK	-	-	-	-	-	GP1_23	3.3V(VCCQ)/4mA
	I(I)	I	I	-	-	-	-	-	IO(I)	On
214	LBSC	SCIFB1	-	-	-	-	-	-		I(GPIO)
L5	DREQ0#	SCIFB1_RXD	-	-	-	-	-	-	GP1_24	3.3V(VCCQ)/4mA
	I	I	-	-	-	-	-	-	IO(I)	On
215	LBSC	-	-	-	-	-	-	-		I(Mode Pin)
M2	DACK0	-	-	-	-	-	-	-	GP1_25	3.3V(VCCQ)/4mA
MD21	O	-	-	-	-	-	-	-	IO(I)	Off

Note: (No.201): Output value of CS1#/A26 pin after power-on reset is 'H' when MD4 = 0 (area 0: 64-MByte), 'L' when MD4 = 1 (area 0: 128-Mbyte).

DU, SCIF, I2C, SCIFA, RCAN and GPIO (No.216 to 235): Up to 6-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR2 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	GPIO	
No.							During POR
Pin No.							V(power)/|IOH|
							Pull-up
216	DU0	Reserved	SCIF5	I2C2	-		I(GPIO)
AA18	DU0_DR0	-	SCIF5_RXD_C	I2C2_SCL_D	-	GP2_0	3.3V(VCCQ)/8mA
	O	-	I	IO	-	IO(I)	On
217	DU0	Reserved	SCIF5	I2C2	-		I(GPIO)
AB18	DU0_DR1	-	SCIF5_TXD_C	I2C2_SDA_D	-	GP2_1	3.3V(VCCQ)/8mA
	O	-	O	IO	-	IO(I)	On
218	DU0	Reserved	-	-	-		I(GPIO)
AE19	DU0_DR2	-	-	-	-	GP2_2	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
219	DU0	Reserved	-	-	-		I(GPIO)
AC18	DU0_DR3	-	-	-	-	GP2_3	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
220	DU0	Reserved	-	-	-		I(GPIO)
AD19	DU0_DR4	-	-	-	-	GP2_4	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
221	DU0	Reserved	-	-	-		I(GPIO)
AD17	DU0_DR5	-	-	-	-	GP2_5	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
222	DU0	Reserved	-	-	-		I(GPIO)
AC17	DU0_DR6	-	-	-	-	GP2_6	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
223	DU0	Reserved	-	-	-		I(GPIO)
AC19	DU0_DR7	-	-	-	-	GP2_7	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
224	DU0	Reserved	SCIFA0	I2C3	-		I(GPIO)
AA17	DU0_DG0	-	SCIFA0_RXD_C	I2C3_SCL_D	-	GP2_8	3.3V(VCCQ)/8mA
	O	-	I	IO	-	IO(I)	On
225	DU0	Reserved	SCIFA0	I2C3	-		I(GPIO)
AB16	DU0_DG1	-	SCIFA0_TXD_C	I2C3_SDA_D	-	GP2_9	3.3V(VCCQ)/8mA
	O	-	O	IO	-	IO(I)	On
226	DU0	Reserved	-	-	-		I(GPIO)
AD18	DU0_DG2	-	-	-	-	GP2_10	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
227	DU0	Reserved	-	-	-		I(GPIO)
AD16	DU0_DG3	-	-	-	-	GP2_11	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
228	DU0	Reserved	-	-	-		I(GPIO)
AB17	DU0_DG4	-	-	-	-	GP2_12	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
229	DU0	Reserved	-	-	-		I(GPIO)
AA16	DU0_DG5	-	-	-	-	GP2_13	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
230	DU0	Reserved	-	-	-		I(GPIO)
AE16	DU0_DG6	-	-	-	-	GP2_14	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
231	DU0	Reserved	-	-	-		I(GPIO)
AC16	DU0_DG7	-	-	-	-	GP2_15	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
232	DU0	Reserved	SCIFA4	I2C4	RCAN0		I(GPIO)
AC14	DU0_DB0	-	SCIFA4_RXD_C	I2C4_SCL_D	CAN0_RX_C	GP2_16	3.3V(VCCQ)/8mA
	O	-	I	IO	I	IO(I)	On
233	DU0	Reserved	SCIFA4	I2C4	RCAN0		I(GPIO)
AE17	DU0_DB1	-	SCIFA4_TXD_C	I2C4_SDA_D	CAN0_TX_C	GP2_17	3.3V(VCCQ)/8mA
	O	-	O	IO	O	IO(I)	On
234	DU0	Reserved	-	-	-		I(GPIO)
AA15	DU0_DB2	-	-	-	-	GP2_18	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On
235	DU0	Reserved	-	-	-		I(GPIO)
AB15	DU0_DB3	-	-	-	-	GP2_19	3.3V(VCCQ)/8mA
	O	-	-	-	-	IO(I)	On

DU, VIN, EtherAVB and GPIO (No.236 to 256): Up to 3-Function Multiplexed and Mode Pin assigned (No.243, 244, 246 and 247)

These pins are set for GPIO after power-on reset. For details, refer to GPSR2 and GPSR3 registers in section 5, Pin Function Controller (PFC).

Function	1	2	GPIO	
No.	Module	-		During POR
Pin No.	Pin Name	-		V(power)/|IOH|
Mode Pin	I/O	-		Pull-up
236	DU0	Reserved		I(GPIO)
AD14	DU0_DB4	-	GP2_20	3.3V(VCCQ)/8mA
	O	-	IO(I)	On
237	DU0	Reserved		I(GPIO)
AD15	DU0_DB5	-	GP2_21	3.3V(VCCQ)/8mA
	O	-	IO(I)	On
238	DU0	Reserved		I(GPIO)
AA14	DU0_DB6	-	GP2_22	3.3V(VCCQ)/8mA
	O	-	IO(I)	On
239	DU0	Reserved		I(GPIO)
AC15	DU0_DB7	-	GP2_23	3.3V(VCCQ)/8mA
	O	-	IO(I)	On
240	DU0	Reserved		I(GPIO)
AE15	DU0_DOTCLKIN	-	GP2_24	3.3V(VCCQ)/8mA
	I	-	IO(I)	On
241	DU0	Reserved		I(GPIO)
AE14	DU0_DOTCLKOUT0	-	GP2_25	3.3V(VCCQ)/8mA
	O	-	IO(I)	On
242	DU0	Reserved		I(GPIO)
AE13	DU0_DOTCLKOUT1	-	GP2_26	3.3V(VCCQ)/8mA
	O	-	IO(I)	On
243	DU0	Reserved		I(Mode Pin)
AD13	DU0_EXHSYNC/DU0_HSYNC	-	GP2_27	3.3V(VCCQ)/8mA
MD11	IO	-	IO(I)	Off
244	DU0	Reserved		I(Mode Pin)
AB14	DU0_EXVSYNC/DU0_VSYNC	-	GP2_28	3.3V(VCCQ)/8mA
MD12	IO	-	IO(I)	Off
245	DU0	Reserved		I(GPIO)
AC13	DU0_EXODDF/DU0_ODDF/DISP/CDE	-	GP2_29	3.3V(VCCQ)/8mA
	IO	-	IO(I)	On
246	DU0	Reserved		I(Mode Pin)
AE18	DU0_DISP	-	GP2_30	3.3V(VCCQ)/8mA
MD10	O	-	IO(I)	Off
247	DU0	Reserved		I(Mode Pin)
AB13	DU0_CDE	-	GP2_31	3.3V(VCCQ)/8mA
MD13	O	-	IO(I)	Off
248	VIN0	EthernetAVB		I(GPIO)
AB1	VI0_CLK	AVB_RX_CLK	GP3_0	3.3V(VCCQ)/4mA
	I	I	IO(I)	On
249	VIN0	EthernetAVB		I(GPIO)
AA4	VI0_DATA0/VI0_B0	AVB_RX_DV	GP3_1	3.3V(VCCQ)/4mA
	I	I	IO(I)	On
250	VIN0	EthernetAVB		I(GPIO)
AB3	VI0_DATA1/VI0_B1	AVB_RXD0	GP3_2	3.3V(VCCQ)/4mA
	I	I	IO(I)	On
251	VIN0	EthernetAVB		I(GPIO)
AA3	VI0_DATA2/VI0_B2	AVB_RXD1	GP3_3	3.3V(VCCQ)/4mA
	I	I	IO(I)	On
252	VIN0	EthernetAVB		I(GPIO)
AB2	VI0_DATA3/VI0_B3	AVB_RXD2	GP3_4	3.3V(VCCQ)/4mA
	I	I	IO(I)	On
253	VIN0	EthernetAVB		I(GPIO)
Y3	VI0_DATA4/VI0_B4	AVB_RXD3	GP3_5	3.3V(VCCQ)/4mA
	I	I	IO(I)	On
254	VIN0	EthernetAVB		I(GPIO)
W3	VI0_DATA5/VI0_B5	AVB_RXD4	GP3_6	3.3V(VCCQ)/4mA
	I	I	IO(I)	On
255	VIN0	EthernetAVB		I(GPIO)
Y2	VI0_DATA6/VI0_B6	AVB_RXD5	GP3_7	3.3V(VCCQ)/4mA
	I	I	IO(I)	On
256	VIN0	EthernetAVB		I(GPIO)
AA2	VI0_DATA7/VI0_B7	AVB_RXD6	GP3_8	3.3V(VCCQ)/4mA
	I	I	IO(I)	On

VIN, I2C, SCIFA, EthernetAVB, ADG, EtherMAC, MSIOF, RCAN, SCIF, IIC, SSI, HSCIF and GPIO (No.257 to 277): Up to 8-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	GPIO	
No.									During POR
Pin No.									V(power)/|IOH|
									Pull-up
257	VIN0	I2C3	SCIFA5	Reserved	EthernetAVB	-	-		I(GPIO)
AA1	VI0_CLKENB	I2C3_SCL	SCIFA5_RXD_C	-	AVB_RXD7	-	-	GP3_9	3.3V(VCCQ)/4mA
	I	IO	I	-	I	-	-	IO(I)	On
258	VIN0	I2C3	SCIFA5	Reserved	EthernetAVB	-	-		I(GPIO)
W2	VI0_FIELD	I2C3_SDA	SCIFA5_TXD_C	-	AVB_RX_ER	-	-	GP3_10	3.3V(VCCQ)/4mA
	I	IO	O	-	I	-	-	IO(I)	On
259	VIN0	SCIF0	I2C0	Reserved	EthernetAVB	-	-		I(GPIO)
Y1	VI0_HSYNC#	SCIF0_RXD_B	I2C0_SCL_C	-	AVB_COL	-	-	GP3_11	3.3V(VCCQ)/4mA
	I	I	IO	-	I	-	-	IO(I)	On
260	VIN0	SCIF0	I2C0	ADG	EthernetAVB	-	-		I(GPIO)
W1	VI0_VSYNC#	SCIF0_TXD_B	I2C0_SDA_C	AUDIO_CLKOUT_B	AVB_TX_EN	-	-	GP3_12	3.3V(VCCQ)/8mA
	I	O	IO	O	O	-	-	IO(I)	On
261	EtherMAC	VIN0	MSIOF2	I2C5	EthernetAVB	Reserved	Reserved		I(GPIO)
T5	ETH_MDIO	VI0_G0	MSIOF2_RXD_B	I2C5_SCL_D	AVB_TX_CLK	-	-	GP3_13	3.3V(VCCQ)/4mA
	IO	I	I	IO	I	-	-	IO(I)	On
262	EtherMAC	VIN0	MSIOF2	I2C5	EthernetAVB	Reserved	Reserved		I(GPIO)
V4	ETH_CRS_DV	VI0_G1	MSIOF2_TXD_B	I2C5_SDA_D	AVB_TXD0	-	-	GP3_14	3.3V(VCCQ)/8mA
	I	I	O	IO	O	-	-	IO(I)	On
263	EtherMAC	VIN0	MSIOF2	RCAN0	EthernetAVB	Reserved	Reserved		I(GPIO)
U5	ETH_RX_ER	VI0_G2	MSIOF2_SCK_B	CAN0_RX_B	AVB_TXD1	-	-	GP3_15	3.3V(VCCQ)/8mA
	I	I	IO	I	O	-	-	IO(I)	On
264	EtherMAC	VIN0	MSIOF2	RCAN0	EthernetAVB	Reserved	Reserved		I(GPIO)
V3	ETH_RXD0	VI0_G3	MSIOF2_SYNC_B	CAN0_TX_B	AVB_TXD2	-	-	GP3_16	3.3V(VCCQ)/8mA
	I	I	IO	O	O	-	-	IO(I)	On
265	EtherMAC	VIN0	MSIOF2	SCIF4	EthernetAVB	Reserved	-		I(GPIO)
U4	ETH_RXD1	VI0_G4	MSIOF2_SS1_B	SCIF4_RXD_D	AVB_TXD3	-	-	GP3_17	3.3V(VCCQ)/8mA
	I	I	O	I	O	-	-	IO(I)	On
266	EtherMAC	VIN0	MSIOF2	SCIF4	EthernetAVB	Reserved	-		I(GPIO)
V5	ETH_LINK	VI0_G5	MSIOF2_SS2_B	SCIF4_TXD_D	AVB_TXD4	-	-	GP3_18	3.3V(VCCQ)/8mA
	I	I	O	O	O	-	-	IO(I)	On
267	EtherMAC	VIN0	SCIF2	EthernetAVB	SSI	-	-		I(GPIO)
V1	ETH_REF_CLK	VI0_G6	SCIF2_SCK_C	AVB_TXD5	SSI_SCK5_B	-	-	GP3_19	3.3V(VCCQ)/8mA
	I	I	IO	O	IO	-	-	IO(I)	On
268	EtherMAC	VIN0	SCIF2	IIC0 (I2C6)	EthernetAVB	SSI	-		I(GPIO)
V2	ETH_TXD1	VI0_G7	SCIF2_RXD_C	IIC0_SCL_D	AVB_TXD6	SSI_WS5_B	-	GP3_20	3.3V(VCCQ)/8mA
	O	I	I	IO	O	IO	-	IO(I)	On
269	EtherMAC	VIN0	SCIF2	IIC0 (I2C6)	EthernetAVB	SSI	-		I(GPIO)
U3	ETH_TX_EN	VI0_R0	SCIF2_TXD_C	IIC0_SDA_D	AVB_TXD7	SSI_SDATA5_B	-	GP3_21	3.3V(VCCQ)/8mA
	O	I	O	IO	O	IO	-	IO(I)	On
270	EtherMAC	VIN0	SCIF3	EthernetAVB	SSI	-	-		I(GPIO)
W4	ETH_MAGIC	VI0_R1	SCIF3_SCK_B	AVB_TX_ER	SSI_SCK6_B	-	-	GP3_22	3.3V(VCCQ)/8mA
	O	I	IO	O	IO	-	-	IO(I)	On
271	EtherMAC	VIN0	SCIF3	I2C4	EthernetAVB	SSI	-		I(GPIO)
U2	ETH_TXD0	VI0_R2	SCIF3_RXD_B	I2C4_SCL_E	AVB_GTX_CLK	SSI_WS6_B	-	GP3_23	3.3V(VCCQ)/8mA
	O	I	I	IO	O	IO	-	IO(I)	On
272	EtherMAC	VIN0	SCIF3	I2C4	EthernetAVB	SSI	-		I(GPIO)
W5	ETH_MDC	VI0_R3	SCIF3_TXD_B	I2C4_SDA_E	AVB_MDC	SSI_SDATA6_B	-	GP3_24	3.3V(VCCQ)/8mA
	O	I	O	IO	O	IO	-	IO(I)	On
273	HSCIF0	VIN0	I2C1	ADG	EthernetAVB	SSI	-		I(GPIO)
U1	HSCIF0_HRX	VI0_R4	I2C1_SCL_C	AUDIO_CLKA_B	AVB_MDIO	SSI_SCK78_B	-	GP3_25	3.3V(VCCQ)/8mA
	I	I	IO	I	IO	IO	-	IO(I)	On
274	HSCIF0	VIN0	I2C1	ADG	EthernetAVB	SSI	-		I(GPIO)
T4	HSCIF0_HTX	VI0_R5	I2C1_SDA_C	AUDIO_CLKB_B	AVB_LINK	SSI_WS78_B	-	GP3_26	3.3V(VCCQ)/8mA
	O	I	IO	I	I	IO	-	IO(I)	On
275	HSCIF0	VIN0	SCIF0	I2C0	EthernetAVB	SSI	-		I(GPIO)
T3	HSCIF0_HCTS#	VI0_R6	SCIF0_RXD_D	I2C0_SCL_E	AVB_MAGIC	SSI_SDATA7_B	-	GP3_27	3.3V(VCCQ)/8mA
	IO	I	I	IO	O	IO	-	IO(I)	On
276	HSCIF0	VIN0	SCIF0	I2C0	EthernetAVB	SSI	-		I(GPIO)
T2	HSCIF0_HRTS#	VI0_R7	SCIF0_TXD_D	I2C0_SDA_E	AVB_PHY_INT	SSI_SDATA8_B	-	GP3_28	3.3V(VCCQ)/8mA
	IO	I	O	IO	I	IO	-	IO(I)	On
277	HSCIF0	SCIF	EthernetAVB	ADG	-	-	-		I(GPIO)
T1	HSCIF0_HSCK	SCIF_CLK_B	AVB_CRS	AUDIO_CLKC_B	-	-	-	GP3_29	3.3V(VCCQ)/8mA
	IO	I	I	I	-	-	-	IO(I)	On

I2C, SCIF, PWM, TMU, EthernetAVB, RCAN, TPU, SCU, DU, INTC, MSIOF, SCIFA, HSCIF, SSI, IIC and GPIO (No.278 to 298): Up to 9-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR3 and GPSR4 registers in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	GPIO	
No.										During POR
Pin No.										V(power)/|IOH|
										Pull-up
278	I2C0	SCIF0	PWM5	TMU	EthernetAVB	RCAN1	TPU	-		I(GPIO)
Y5	I2C0_SCL	SCIF0_RXD_C	PWM5	TCLK1_B	AVB_GTXREFCLK	CAN1_RX_D	TPUTO0_B	-	GP3_30	3.3V(VCCQ)/8mA
	IO	I	O	I	I	I	O	-	IO(I)	On
279	I2C0	SCIF0	TPU	RCAN	SCU	RCAN1	-	-		I(GPIO)
Y4	I2C0_SDA	SCIF0_TXD_C	TPUTO0	CAN_CLK	DVC_MUTE	CAN1_TX_D	-	-	GP3_31	3.3V(VCCQ)/8mA
	IO	O	O	I	I	O	-	-	IO(I)	On
280	I2C1	SCIF4	PWM5	DU1	Reserved	Reserved	TPU	-		I(GPIO)
Y24	I2C1_SCL	SCIF4_RXD	PWM5_B	DU1_DR0	-	-	TPUTO1_B	-	GP4_0	3.3V(VCCQ)/8mA
	IO	I	O	O	-	-	O	-	IO(I)	On
281	I2C1	SCIF4	INTC	DU1	Reserved	Reserved	Reserved	-		I(GPIO)
Y25	I2C1_SDA	SCIF4_TXD	IRQ5	DU1_DR1	-	-	-	-	GP4_1	3.3V(VCCQ)/8mA
	IO	O	I	O	-	-	-	-	IO(I)	On
282	MSIOF0	SCIF5	I2C2	DU1	Reserved	Reserved	Reserved	Reserved		I(GPIO)
W24	MSIOF0_RXD	SCIF5_RXD	I2C2_SCL_C	DU1_DR2	-	-	-	-	GP4_2	3.3V(VCCQ)/8mA
	I	I	IO	O	-	-	-	-	IO(I)	On
283	MSIOF0	SCIF5	I2C2	DU1	Reserved	Reserved	Reserved	Reserved		I(GPIO)
W23	MSIOF0_TXD	SCIF5_TXD	I2C2_SDA_C	DU1_DR3	-	-	-	-	GP4_3	3.3V(VCCQ)/8mA
	O	O	IO	O	-	-	-	-	IO(I)	On
284	MSIOF0	INTC	Reserved	DU1	Reserved	TPU	-	-		I(GPIO)
AA25	MSIOF0_SCK	IRQ0	-	DU1_DR4	-	TPUTO1_C	-	-	GP4_4	3.3V(VCCQ)/8mA
	IO	I	-	O	-	O	-	-	IO(I)	On
285	MSIOF0	PWM1	Reserved	DU1	Reserved	Reserved	Reserved	-		I(GPIO)
AB25	MSIOF0_SYNC	PWM1	-	DU1_DR5	-	-	-	-	GP4_5	3.3V(VCCQ)/8mA
	IO	O	-	O	-	-	-	-	IO(I)	On
286	MSIOF0	SCIFA0	Reserved	DU1	Reserved	Reserved	Reserved	-		I(GPIO)
Y22	MSIOF0_SS1	SCIFA0_RXD	-	DU1_DR6	-	-	-	-	GP4_6	3.3V(VCCQ)/8mA
	O	I	-	O	-	-	-	-	IO(I)	On
287	MSIOF0	SCIFA0	Reserved	DU1	Reserved	Reserved	-	-		I(GPIO)
W22	MSIOF0_SS2	SCIFA0_TXD	-	DU1_DR7	-	-	-	-	GP4_7	3.3V(VCCQ)/8mA
	O	O	-	O	-	-	-	-	IO(I)	On
288	HSCIF1	I2C4	PWM6	DU1	-	-	-	-		I(GPIO)
AB23	HSCIF1_HRX	I2C4_SCL	PWM6	DU1_DG0	-	-	-	-	GP4_8	3.3V(VCCQ)/8mA
	I	IO	O	O	-	-	-	-	IO(I)	On
289	HSCIF1	I2C4	TPU	DU1	-	-	Reserved	-		I(GPIO)
AA23	HSCIF1_HTX	I2C4_SDA	TPUTO1	DU1_DG1	-	-	-	-	GP4_9	3.3V(VCCQ)/8mA
	O	IO	O	O	-	-	-	-	IO(I)	On
290	HSCIF1	PWM2	Reserved	DU1	Reserved	Reserved	-	-		I(GPIO)
AA24	HSCIF1_HSCK	PWM2	-	DU1_DG2	-	-	-	-	GP4_10	3.3V(VCCQ)/8mA
	IO	O	-	O	-	-	-	-	IO(I)	On
291	HSCIF1	SCIFA4	Reserved	DU1	SSI	-	-	-		I(GPIO)
Y23	HSCIF1_HCTS#	SCIFA4_RXD	-	DU1_DG3	SSI_SCK1_B	-	-	-	GP4_11	3.3V(VCCQ)/8mA
	IO	I	-	O	IO	-	-	-	IO(I)	On
292	HSCIF1	SCIFA4	Reserved	DU1	SSI	-	-	-		I(GPIO)
AB24	HSCIF1_HRTS#	SCIFA4_TXD	-	DU1_DG4	SSI_WS1_B	-	-	-	GP4_12	3.3V(VCCQ)/8mA
	IO	O	-	O	IO	-	-	-	IO(I)	On
293	SCIF1	PWM3	TMU	DU1	SSI	-	-	-		I(GPIO)
AC25	SCIF1_SCK	PWM3	TCLK2	DU1_DG5	SSI_SDATA1_B	-	-	-	GP4_13	3.3V(VCCQ)/8mA
	IO	O	I	O	IO	-	-	-	IO(I)	On
294	SCIF1	I2C5	DU1	SSI	-	-	-	-		I(GPIO)
AD25	SCIF1_RXD	I2C5_SCL	DU1_DG6	SSI_SCK2_B	-	-	-	-	GP4_14	3.3V(VCCQ)/8mA
	I	IO	O	IO	-	-	-	-	IO(I)	On
295	SCIF1	I2C5	DU1	SSI	-	-	-	-		I(GPIO)
AC24	SCIF1_TXD	I2C5_SDA	DU1_DG7	SSI_WS2_B	-	-	-	-	GP4_15	3.3V(VCCQ)/8mA
	O	IO	O	IO	-	-	-	-	IO(I)	On
296	SCIF2	IIC0 (I2C6)	DU1	SSI	Reserved	-	-	-		I(GPIO)
AD23	SCIF2_RXD	IIC0_SCL	DU1_DB0	SSI_SDATA2_B	-	-	-	-	GP4_16	3.3V(VCCQ)/8mA
	I	IO	O	IO	-	-	-	-	IO(I)	On
297	SCIF2	IIC0 (I2C6)	DU1	SSI	Reserved	-	-	-		I(GPIO)
AE23	SCIF2_TXD	IIC0_SDA	DU1_DB1	SSI_SCK9_B	-	-	-	-	GP4_17	3.3V(VCCQ)/8mA
	O	IO	O	IO	-	-	-	-	IO(I)	On
298	SCIF2	INTC	DU1	SSI	Reserved	-	TPU	-		I(GPIO)
AE24	SCIF2_SCK	IRQ1	DU1_DB2	SSI_WS9_B	-	-	TPUTO0_B	-	GP4_18	3.3V(VCCQ)/8mA
	IO	I	O	IO	-	-	O	-	IO(I)	On

SCIF, INTC, DU, SSI, I2C, ADG, SCIFA, RCAN, MSIOF, PWM, LBSC and GPIO (No.299 to 318): Up to 9-Function Multiplexed

These pins are set for GPIO after power-on reset. For details, refer to GPSR4 and GPSR5 registers in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	GPIO	
No.										During POR
Pin No.										V(power)/|IOH|
										Pull-up
299	SCIF3	INTC	Reserved	DU1	SSI	Reserved	-	-		I(GPIO)
AA22	SCIF3_SCK	IRQ2	-	DU1_DB3	SSI_SDATA9_B	-	-	-	GP4_19	3.3V(VCCQ)/8mA
	IO	I	-	O	IO	-	-	-	IO(I)	On
300	SCIF3	I2C1	Reserved	DU1	ADG	SSI	-	Reserved		I(GPIO)
AC22	SCIF3_RXD	I2C1_SCL_E	-	DU1_DB4	AUDIO_CLKA_C	SSI_SCK4_B	-	-	GP4_20	3.3V(VCCQ)/8mA
	I	IO	-	O	I	IO	-	-	IO(I)	On
301	SCIF3	I2C1	Reserved	DU1	ADG	SSI	-	Reserved		I(GPIO)
AC21	SCIF3_TXD	I2C1_SDA_E	-	DU1_DB5	AUDIO_CLKB_C	SSI_WS4_B	-	-	GP4_21	3.3V(VCCQ)/8mA
	O	IO	-	O	I	IO	-	-	IO(I)	On
302	I2C2	SCIFA5	DU1	ADG	SSI	-	-	-		I(GPIO)
AD21	I2C2_SCL	SCIFA5_RXD	DU1_DB6	AUDIO_CLKC_C	SSI_SDATA4_B	-	-	-	GP4_22	3.3V(VCCQ)/8mA
	IO	I	O	I	IO	-	-	-	IO(I)	On
303	I2C2	SCIFA5	DU1	ADG	-	-	-	-		I(GPIO)
AC20	I2C2_SDA	SCIFA5_TXD	DU1_DB7	AUDIO_CLKOUT_C	-	-	-	-	GP4_23	3.3V(VCCQ)/8mA
	IO	O	O	O	-	-	-	-	IO(I)	On
304	SSI	SCIFA3	DU1	-	-	-	-	-		I(GPIO)
AE22	SSI_SCK5	SCIFA3_SCK	DU1_DOTCLKIN	-	-	-	-	-	GP4_24	3.3V(VCCQ)/8mA
	IO	O	I	-	-	-	-	-	IO(I)	On
305	SSI	SCIFA3	I2C3	DU1	-	-	-	-		I(GPIO)
AB20	SSI_WS5	SCIFA3_RXD	I2C3_SCL_C	DU1_DOTCLKOUT0	-	-	-	-	GP4_25	3.3V(VCCQ)/8mA
	IO	I	IO	O	-	-	-	-	IO(I)	On
306	SSI	SCIFA3	I2C3	DU1	-	-	-	-		I(GPIO)
AA20	SSI_SDATA5	SCIFA3_TXD	I2C3_SDA_C	DU1_DOTCLKOUT1	-	-	-	-	GP4_26	3.3V(VCCQ)/8mA
	IO	O	IO	O	-	-	-	-	IO(I)	On
307	SSI	SCIFA1	DU1	-	-	-	-	-		I(GPIO)
AE20	SSI_SCK6	SCIFA1_SCK_B	DU1_EXHSYNC /DU1_HSYNC	-	-	-	-	-	GP4_27	3.3V(VCCQ)/8mA
	IO	O	IO	-	-	-	-	-	IO(I)	On
308	SSI	SCIFA1	I2C4	DU1	-	-	-	-		I(GPIO)
AD20	SSI_WS6	SCIFA1_RXD_B	I2C4_SCL_C	DU1_EXVSYNC/DU 1_VSYNC	-	-	-	-	GP4_28	3.3V(VCCQ)/8mA
	IO	I	IO	IO	-	-	-	-	IO(I)	On
309	SSI	SCIFA1	I2C4	DU1	-	-	-	-		I(GPIO)
AE21	SSI_SDATA6	SCIFA1_TXD_B	I2C4_SDA_C	DU1_EXODDF/DU1 _ODDF/DISP/CDE	-	-	-	-	GP4_29	3.3V(VCCQ)/8mA
	IO	O	IO	IO	-	-	-	-	IO(I)	On
310	SSI	SCIFA2	I2C5	DU1	-	-	-	-		I(GPIO)
AB19	SSI_SCK78	SCIFA2_SCK_B	I2C5_SDA_C	DU1_DISP	-	-	-	-	GP4_30	3.3V(VCCQ)/8mA
	IO	O	IO	O	-	-	-	-	IO(I)	On
311	SSI	SCIFA2	I2C5	DU1	-	-	-	-		I(GPIO)
AA19	SSI_WS78	SCIFA2_RXD_B	I2C5_SCL_C	DU1_CDE	-	-	-	-	GP4_31	3.3V(VCCQ)/8mA
	IO	I	IO	O	-	-	-	-	IO(I)	On
312	SSI	SCIFA2	INTC	ADG	RCAN	-	-	-		I(GPIO)
AB7	SSI_SDATA7	SCIFA2_TXD_B	IRQ8	AUDIO_CLKA_D	CAN_CLK_D	-	-	-	GP5_0	3.3V(VCCQ)/8mA
	IO	O	I	I	I	-	-	-	IO(I)	On
313	SSI	MSIOF1	SCIF5	Reserved	Reserved	-	-	-		I(GPIO)
AE5	SSI_SCK0129	MSIOF1_RXD_B	SCIF5_RXD_D	-	-	-	-	-	GP5_1	3.3V(VCCQ)/8mA
	IO	I	I	-	-	-	-	-	IO(I)	On
314	SSI	MSIOF1	SCIF5	Reserved	Reserved	-	-	-		I(GPIO)
AA7	SSI_WS0129	MSIOF1_TXD_B	SCIF5_TXD_D	-	-	-	-	-	GP5_2	3.3V(VCCQ)/8mA
	IO	O	O	-	-	-	-	-	IO(I)	On
315	SSI	MSIOF1	PWM0	Reserved	Reserved	-	-	-		I(GPIO)
AA6	SSI_SDATA0	MSIOF1_SCK_B	PWM0_B	-	-	-	-	-	GP5_3	3.3V(VCCQ)/8mA
	IO	IO	O	-	-	-	-	-	IO(I)	On
316	SSI	MSIOF1	SCIFA1	Reserved	Reserved	LBSC	-	-		I(GPIO)
AD6	SSI_SCK34	MSIOF1_SYNC_B	SCIFA1_SCK_C	-	-	DREQ1#_B	-	-	GP5_4	3.3V(VCCQ)/8mA
	IO	IO	O	-	-	I	-	-	IO(I)	On
317	SSI	MSIOF1	SCIFA1	Reserved	RCAN1	LBSC	-	-		I(GPIO)
AB6	SSI_WS34	MSIOF1_SS1_B	SCIFA1_RXD_C	-	CAN1_RX_C	DACK1_B	-	-	GP5_5	3.3V(VCCQ)/8mA
	IO	O	I	-	I	O	-	-	IO(I)	On
318	SSI	MSIOF1	SCIFA1	Reserved	RCAN1	LBSC	-	-		I(GPIO)
AD5	SSI_SDATA3	MSIOF1_SS2_B	SCIFA1_TXD_C	-	CAN1_TX_C	DREQ2#	-	-	GP5_6	3.3V(VCCQ)/8mA
	IO	O	O	-	O	I	-	-	IO(I)	On

SSI, SCIF, PWM, INTC, LBSC, EtherMAC, IIC, VIN, RCAN, HSCIF, SCIFA, I2C and GPIO (No.319 to 334): Up to 9-Function Multiplexed

These pins are set for GPIO after power-on reset except for No.322 to 324. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	GPIO	
No.										During POR
Pin No.										V(power)/|IOH|
										Pull-up
319	SSI	Reserved	Reserved	Reserved	-	-	-	-		I(GIPIO)
AD22	SSI_SCK4	-	-	-	-	-	-	-	GP5_7	3.3V(VCCQ)/16mA
	IO	-	-	-	-	-	-	-	IO(I)	-
320	SSI	Reserved	Reserved	Reserved	-	-	-	-		I(GIPIO)
AB21	SSI_WS4	-	-	-	-	-	-	-	GP5_8	3.3V(VCCQ)/16mA
	IO	-	-	-	-	-	-	-	IO(I)	-
321	SSI	Reserved	Reserved	Reserved	-	-	-	-		I(GIPIO)
Y21	SSI_SDATA4	-	-	-	-	-	-	-	GP5_9	3.3V(VCCQ)/16mA
	IO	-	-	-	-	-	-	-	IO(I)	-
322	Reserved	-	-	-	-	-	-	-	-	IO(MLB)
AD24	-	-	-	-	-	-	-	-	-	3.3V(VCCQ)/16mA
	-	-	-	-	-	-	-	-	-	-
323	-	-	-	-	-	-	-	-	-	P
W20	VSS_MLBPLL	-	-	-	-	-	-	-	-	GND(VDD_MLBPLL)/-
	P	-	-	-	-	-	-	-	-	-
324	-	-	-	-	-	-	-	-	-	P
V21	VDD_MLBPLL	-	-	-	-	-	-	-	-	1.8V(VDD_MLBPLL)/-
	P	-	-	-	-	-	-	-	-	-
325	SSI	SCIF1	PWM1	INTC	Reserved	LBSC	EtherMAC	-		I(GPIO)
AC6	SSI_SDATA8	SCIF1_SCK_B	PWM1_B	IRQ9	-	DACK2	ETH_MDIO_B	-	GP5_10	3.3V(VCCQ)/8mA
	IO	IO	O	I	-	O	IO	-	IO(I)	On
326	SSI	SCIF1	IIC0(I2C6)	VIN1	RCAN0	Reserved	EtherMAC	-		I(GPIO)
AE6	SSI_SCK1	SCIF1_RXD_B	IIC0_SCL_C	VI1_CLK	CAN0_RX_D	-	ETH_CRS_DV_B	-	GP5_11	3.3V(VCCQ)/8mA
	IO	I	IO	I	I	-	I	-	IO	On
327	SSI	SCIF1	IIC0(I2C6)	VIN1	RCAN0	Reserved	EtherMAC	-		I(GPIO)
AB5	SSI_WS1	SCIF1_TXD_B	IIC0_SDA_C	VI1_DATA0	CAN0_TX_D	-	ETH_RX_ER_B	-	GP5_12	3.3V(VCCQ)/8mA
	IO	O	IO	I	O	-	I	-	IO	On
328	SSI	HSCIF1	VIN1	Reserved	LBSC	EtherMAC	-	-		I(GPIO)
AC5	SSI_SDATA1	HSCIF1_HRX_B	VI1_DATA1	-	ATAWR0#	ETH_RXD0_B	-	-	GP5_13	3.3V(VCCQ)/8mA
	IO	I	I	-	O	I	-	-	IO	On
329	SSI	HSCIF1	VIN1	Reserved	LBSC	EtherMAC	-	-		I(GPIO)
AE4	SSI_SCK2	HSCIF1_HTX_B	VI1_DATA2	-	ATAG0#	ETH_RXD1_B	-	-	GP5_14	3.3V(VCCQ)/8mA
	IO	O	I	-	O	I	-	-	IO	On
330	SSI	HSCIF1	SCIFA0	VIN1	Reserved	LBSC	EtherMAC	-		I(GPIO)
AD4	SSI_WS2	HSCIF1_HCTS#_B	SCIFA0_RXD_D	VI1_DATA3	-	ATACS00#	ETH_LINK_B	-	GP5_15	3.3V(VCCQ)/8mA
	IO	IO	I	I	-	O	I	-	IO	On
331	SSI	HSCIF1	SCIFA0	VIN1	Reserved	LBSC	EtherMAC	-		I(GPIO)
AC4	SSI_SDATA2	HSCIF1_HRTS#_B	SCIFA0_TXD_D	VI1_DATA4	-	ATACS10#	ETH_REF_CLK_B	-	GP5_16	3.3V(VCCQ)/8mA
	IO	IO	O	I	-	O	I	-	IO	On
332	SSI	SCIF2	PWM2	VIN1	Reserved	LBSC	EtherMAC	-		I(GPIO)
AE3	SSI_SCK9	SCIF2_SCK_B	PWM2_B	VI1_DATA5	-	EX_WAIT1	ETH_TXD1_B	-	GP5_17	3.3V(VCCQ)/8mA
	IO	IO	O	I	-	I	O	-	IO	On
333	SSI	SCIF2	I2C3	VIN1	LBSC	EtherMAC	-	-		I(GPIO)
AD3	SSI_WS9	SCIF2_RXD_B	I2C3_SCL_E	VI1_DATA6	ATARD0#	ETH_TX_EN_B	-	-	GP5_18	3.3V(VCCQ)/8mA
	IO	I	IO	I	O	O	-	-	IO	On
334	SSI	SCIF2	I2C3	VIN1	LBSC	EtherMAC	-	-		I(GPIO)
AD2	SSI_SDATA9	SCIF2_TXD_B	I2C3_SDA_E	VI1_DATA7	ATADIR0#	ETH_MAGIC_B	-	-	GP5_19	3.3V(VCCQ)/8mA
	IO	O	IO	I	O	O	-	-	IO	On

ADG, I2C, SCIFA, VIN, EtherMAC, IIC and GPIO (No.335 to 340): Up to 9-Function Multiplexed

These pins are set for GPIO after power-on reset except for No.339 and 340. For details, refer to GPSR5 register in section 5, Pin Function Controller (PFC).

Function	1	2	3	4	5	6	7	8	GPIO	
No.										During POR
Pin No.										V(power)/|IOH|
										Pull-up
335	ADG	I2C0	SCIFA4	VIN1	Reserved	Reserved	EtherMAC	-		I(GPIO)
AD1	AUDIO_CLKA	I2C0_SCL_B	SCIFA4_RXD_D	VI1_CLKENB	-	-	ETH_TXD0_B	-	GP5_20	3.3V(VCCQ)/8mA
	I	IO	I	I	-	-	O	-	IO(I)	On
336	ADG	I2C0	SCIFA4	VIN1	Reserved	Reserved	Reserved	EtherMAC		I(GPIO)
AE2	AUDIO_CLKB	I2C0_SDA_B	SCIFA4_TXD_D	VI1_FIELD	-	-	-	ETH_MDC_B	GP5_21	3.3V(VCCQ)/8mA
	I	IO	O	I	-	-	-	O	IO(I)	On
337	ADG	I2C4	SCIFA5	VIN1	Reserved	Reserved	Reserved	Reserved		I(GPIO)
AC1	AUDIO_CLKC	I2C4_SCL_B	SCIFA5_RXD_D	VI1_HSYNC#	-	-	-	-	GP5_22	3.3V(VCCQ)/8mA
	I	IO	I	I	-	-	-	-	IO(I)	On
338	ADG	I2C4	SCIFA5	VIN1	Reserved	Reserved	Reserved	Reserved		I(GPIO)
AC2	AUDIO_CLKOUT	I2C4_SDA_B	SCIFA5_TXD_D	VI1_VSYNC#	-	-	-	-	GP5_23	3.3V(VCCQ)/8mA
	O	IO	O	I	-	-	-	-	IO(I)	On
339	IIC1	-	-	-	-	-	-	-	-	Z
W21	IIC1_SCL	-	-	-	-	-	-	-	-	1.8V(VCCQ18)*/-
	IO(OD, Z)	-	-	-	-	-	-	-	-	-
340	IIC1	-	-	-	-	-	-	-	-	Z
V22	IIC1_SDA	-	-	-	-	-	-	-	-	1.8V(VCCQ18)*/-
	IO(OD, Z)	-	-	-	-	-	-	-	-	-

Note: No.339 and 340 (IIC1_SCL and IIC1_SDA) pin voltage: Input/output 3.3V tolerant pins
When using these pins as 3.3 V tolerant, all the external pull-up power supply for these pins must be kept the same power on/off sequence as the VCCQ of this LSI.

- End of Table 4.1 -

4.2 Pin States

Table 4.2 is pin state of the RZ/G1E.

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Pin Name: Pin name of function 1 in pin in Table 4.1,
I/O: Input or output direction of the pin name column pin (function 1).

I: Input, IO: Input and output, O: Output, -: N/A.

During POR: Pin state during power-on reset (PRESET# pin input is low-level).

Default Pin Function: Pin function after power-on reset

Default State: Pin state of default pin function

I: Input, I(S): Schmitt input, IO: Input and output, IO (OD): Input and open drain output, O: Output, P: Power supply pin.

(I)/(H)/(L)/(X)/(Z) with I, O or IO: Default pin state

H: High level output, L: Low level output, X: Undefined value output, Z: High impedance

Default pull-up: Internal pull-up control function is available or not from a power-on reset and its pull-up state.

"On": Pull-up control function is available and default state is pulled-up.

(No.110, ACK pin is available internal pull-down function.)

"Off": Pull-up control function is available and default state is not pulled-up.

"-": Pull-up control function is not available.

For details of pull-up control function, refer to PUPR0 through PUPR12 registers in section 5, Pin Function Controller (PFC).

Notes: 1. All power supply pins and ground pins include VCCQ, VCCQ18, VDD, VDDQ_M0, VDDQ_M0BKUP, and VSS pins which are not listed in Table 4.2 must be used.

2. All mode pins must be used during power-on reset. For details of mode pin settings, refer to section 3.3, Mode Pin Settings.
3. Boot module related pins (LBSC area 0 or QSPI) should be used during boot operation. For details of QSPI boot, refer to section 18, Booting.
4. For multiplexed pins and modules of each pin, refer to Table 4.1.

Table 4.2 Pin States

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
1	D15	M0CKE0	O	X	M0CKE0	O(L)	-
2	E11	M0CKE1	O	X	M0CKE1	O(L)	-
3	D14	M0VREFCA	-	P	-	P	-
4	E7	M0BKPRST#	I	I	M0BKPRST#	I	-
5	D12	M0RESET#	O	H	M0RESET#	H to L	-
6	A15	M0CK0	O	X	M0CK0	O	-
7	A14	M0CK0#	O	X	M0CK0#	O	-
8	C11	M0CK1	O	X	M0CK1	O	-
9	C10	M0CK1#	O	X	M0CK1#	O	-
10	C15	M0CS0#	O	H	M0CS0#	H	-
11	E10	M0CS1#	O	H	M0CS1#	H	-
12	B16	M0ODT0	O	L	M0ODT0	L	-
13	D11	M0ODT1	O	L	M0ODT1	L	-
14	D9	M0ZQ	IO	IO	M0ZQ	IO	-
15	E14	M0WE#	O	H	M0WE#	H	-
16	D16	M0RAS#	O	H	M0RAS#	H	-
17	E13	M0CAS#	O	H	M0CAS#	H	-
18	B9	M0A0	O	L	M0A0	L	-
19	B12	M0A1	O	L	M0A1	L	-
20	A11	M0A2	O	L	M0A2	L	-
21	B10	M0A3	O	L	M0A3	L	-
22	B13	M0A4	O	L	M0A4	L	-
23	B8	M0A5	O	L	M0A5	L	-
24	A7	M0A6	O	L	M0A6	L	-
25	B14	M0A7	O	L	M0A7	L	-
26	D8	M0A8	O	L	M0A8	L	-
27	B11	M0A9	O	L	M0A9	L	-
28	A8	M0A10	O	L	M0A10	L	-
29	A9	M0A11	O	L	M0A11	L	-
30	A6	M0A12	O	L	M0A12	L	-
31	B7	M0A13	O	L	M0A13	L	-
32	D7	M0A14	O	L	M0A14	L	-
33	A12	M0A15	O	L	M0A15	L	-
34	E12	M0BA0	O	L	M0BA0	L	-
35	A10	M0BA1	O	L	M0BA1	L	-
36	D13	M0BA2	O	L	M0BA2	L	-
37	F12	VDDQ_M0APLL	-	P	-	P	-
38	F13	VSSQ_M0APLL	-	P	-	P	-
39	E20	M0DQ0	IO	Z	M0DQ0	Z	-
40	D21	M0DQ1	IO	Z	M0DQ1	Z	-
41	A24	M0DQ2	IO	Z	M0DQ2	Z	-
42	B22	M0DQ3	IO	Z	M0DQ3	Z	-
43	C20	M0DQ4	IO	Z	M0DQ4	Z	-
44	B23	M0DQ5	IO	Z	M0DQ5	Z	-
45	A23	M0DQ6	IO	Z	M0DQ6	Z	-
46	C22	M0DQ7	IO	Z	M0DQ7	Z	-
47	A21	M0DQS0	IO	Z(*1)	M0DQS0	Z(*1)	-
48	A20	M0DQS0#	IO	Z(*1)	M0DQS0#	Z(*1)	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
49	C21	M0DM0	O	Z	M0DM0	Z	-
50	F16	VDDQ_M0DPLL0	-	P	-	P	-
51	F15	VSSQ_M0DPLL0	-	P	-	P	-
52	C14	M0VREFDQ0	-	P	-	P	-
53	B17	M0DQ8	IO	Z	M0DQ8	Z	-
54	D17	M0DQ9	IO	Z	M0DQ9	Z	-
55	B19	M0DQ10	IO	Z	M0DQ10	Z	-
56	B20	M0DQ11	IO	Z	M0DQ11	Z	-
57	D19	M0DQ12	IO	Z	M0DQ12	Z	-
58	E19	M0DQ13	IO	Z	M0DQ13	Z	-
59	B18	M0DQ14	IO	Z	M0DQ14	Z	-
60	E18	M0DQ15	IO	Z	M0DQ15	Z	-
61	A18	M0DQS1	IO	Z(*1)	M0DQS1	Z(*1)	-
62	A17	M0DQS1#	IO	Z(*1)	M0DQS1#	Z(*1)	-
63	D18	M0DM1	O	Z	M0DM1	Z	-
64	E16	VDDQ_M0DPLL1	-	P	-	P	-
65	E15	VSSQ_M0DPLL1	-	P	-	P	-
66	G24	M0DQ16	IO	Z	M0DQ16	Z	-
67	E22	M0DQ17	IO	Z	M0DQ17	Z	-
68	E24	M0DQ18	IO	Z	M0DQ18	Z	-
69	C25	M0DQ19	IO	Z	M0DQ19	Z	-
70	F24	M0DQ20	IO	Z	M0DQ20	Z	-
71	D24	M0DQ21	IO	Z	M0DQ21	Z	-
72	B25	M0DQ22	IO	Z	M0DQ22	Z	-
73	C24	M0DQ23	IO	Z	M0DQ23	Z	-
74	F25	M0DQS2	IO	Z(*1)	M0DQS2	Z(*1)	-
75	E25	M0DQS2#	IO	Z(*1)	M0DQS2#	Z(*1)	-
76	F22	M0DM2	O	Z	M0DM2	Z	-
77	J21	VDDQ_M0DPLL2	-	P	-	P	-
78	H21	VSSQ_M0DPLL2	-	P	-	P	-
79	G23	M0VREFDQ1	-	P	-	P	-
80	J23	M0DQ24	IO	Z	M0DQ24	Z	-
81	K22	M0DQ25	IO	Z	M0DQ25	Z	-
82	H22	M0DQ26	IO	Z	M0DQ26	Z	-
83	L22	M0DQ27	IO	Z	M0DQ27	Z	-
84	J24	M0DQ28	IO	Z	M0DQ28	Z	-
85	L24	M0DQ29	IO	Z	M0DQ29	Z	-
86	K24	M0DQ30	IO	Z	M0DQ30	Z	-
87	L25	M0DQ31	IO	Z	M0DQ31	Z	-
88	H25	M0DQS3	IO	Z(*1)	M0DQS3	Z(*1)	-
89	J25	M0DQS3#	IO	Z(*1)	M0DQS3#	Z(*1)	-
90	J22	M0DM3	O	Z	M0DM3	Z	-
91	J20	VDDQ_M0DPLL3	-	P	-	P	-
92	H20	VSSQ_M0DPLL3	-	P	-	P	-
93	C7	VDDQ_M0BKUP	-	P	-	P	-
94	V25	EXTAL	I	I	EXTAL	I	-
95	V24	XTAL	O	O	XTAL	O	-
96	E8	VDD_CPGPLL0	-	P	-	P	-
97	E9	VSS_CPGPLL0	-	P	-	P	-
98	K15/L15	VDD_CPGPLL1	-	P	-	P	-

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
99	K16/L16	VSS_CPGPLL1	-	P	-	P	-
100	K12/L12	VDD_CPGPLL3	-	P	-	P	-
101	K11/L11	VSS_CPGPLL3	-	P	-	P	-
102	V23	PRESET#	I	I(L)	PRESET#	I	-
103	B6	PRESETOUT#	O	L	PRESETOUT#	L to H	-
104	R21	BSMODE	I	I	BSMODE	I	-
105	N21	TRST#	I	I(L)	TRST#	I	On
106	N22	TCK	I	I	TCK	I	On
107	P21	TMS	I	I	TMS	I	On
108	R22	TDI	I	I	TDI	I	On
109	P22	TDO	O	Z	TDO	Z	-
110	U23	ACK	IO	I	ACK	I	On(pulldown)
111	T25	USB_EXTAL	I	I	USB_EXTAL	I	-
112	T24	USB_XTAL	O	O	USB_XTAL	O	-
113	P20	VD331	-	P	-	P	-
114	R20	VD181	-	P	-	P	-
115	P23	AVDD	-	P	-	P	-
116	M20	AVSS	-	P	-	P	-
117	P24	USB0_DP	IO	I	USB0_DP	I	-
118	P25	USB0_DM	IO	I	USB0_DM	I	-
119	M25	USB0_RREF	-	P	-	P	-
120	U21	USB0_PWEN	O	Z	USB0_PWEN	L	-
121	U22	USB0_OVC	I	I	USB0_OVC	I	-
122	N24	USB1_DP	IO	I	USB1_DP	I	-
123	N25	USB1_DM	IO	I	USB1_DM	I	-
124	M24	USB1_RREF	-	P	-	P	-
125	T21	USB1_PWEN	O	Z	USB1_PWEN	L	-
126	T22	USB1_OVC	I	I	USB1_OVC	I	-
127	R23	NMI	I	I	NMI	I	-
128	AE12	SD0_CLK	O	I	GP6_0	I	-
129	AD12	SD0_CMD	IO	I	GP6_1	I	Off
130	AC11	SD0_DATA0	IO	I	GP6_2	I	Off
131	AD11	SD0_DATA1	IO	I	GP6_3	I	Off
132	AE11	SD0_DATA2	IO	I	GP6_4	I	Off
133	AA12	SD0_DATA3	IO	I	GP6_5	I	Off
134	AB12	SD0_CD	I	I	GP6_6	I	Off
135	AA13	SD0_WP	I	I	GP6_7	I	Off
136	AC12	VCCQ_SD0	-	P	-	P	-
137	AE8	SD1_CLK	O	I/Z(*2)	GP6_8/TDO2(*2)	I/Z(*2)	-
138	AA8	SD1_CMD	IO	I	GP6_9/TRST2#(*2)	I	Off/-(*3)
139	AD7	SD1_DATA0	IO	I	GP6_10/TCK2(*2)	I	Off/-(*3)
140	AE7	SD1_DATA1	IO	I	GP6_11/TMS2(*2)	I	Off/-(*3)
141	AB8	SD1_DATA2	IO	I	GP6_12/TDI2(*2)	I	Off/-(*3)
142	AC8	SD1_DATA3	IO	I	GP6_13(*2)	I	Off/-(*3)
143	AD8	SD1_CD	I	I	GP6_14	I	Off
144	AE9	SD1_WP	I	I	GP6_15	I	Off
145	AC7	VCCQ_SD1	-	P	-	P	-
146	AE10	MMC_CLK	O	I/Z(*2)	GP6_16/TDO3(*2)	I/Z(*2)	-
147	AD9	MMC_CMD	IO	I	GP6_17/TRST3#(*2)	I	Off/-(*3)
148	AA9	MMC_D0	IO	I	GP6_18/TCK3(*2)	I	Off/-(*3)

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
149	AA11	MMC_D1	IO	I	GP6_19/TMS3(*2)	I	Off/-(*3)
150	AC9	MMC_D2	IO	I	GP6_20/TDI3(*2)	I	Off/-(*3)
151	AA10	MMC_D3	IO	I	GP6_21(*2)	I	Off/-(*3)
152	AB10	MMC_D4	IO	I	GP6_22	I	Off
153	AD10	MMC_D5	IO	I	GP6_23	I	Off
154	AB9	MMC_D6	IO	I	GP6_24	I	Off
155	AB11	MMC_D7	IO	I	GP6_25	I	Off
156	AC10	VCCQ_MMC_SD2	-	P	-	P	-
157	D6	D0	IO	I	D0/GP0_0(*4)	I	On
158	E6	D1	IO	I	D1/GP0_1(*4)	I	On
159	A5	D2	IO	I	D2/GP0_2(*4)	I	On
160	C6	D3	IO	I	D3/GP0_3(*4)	I	On
161	A4	D4	IO	I	D4/GP0_4(*4)	I	On
162	C5	D5	IO	I	D5/GP0_5(*4)	I	On
163	B4	D6	IO	I	D6/GP0_6(*4)	I	On
164	B5	D7	IO	I	D7/GP0_7(*4)	I	On
165	C4	D8	IO	I	D8/GP0_8(*4)	I	On
166	A3	D9	IO	I	D9/GP0_9(*4)	I	On
167	E4	D10	IO	I	D10/GP0_10(*4)	I	On
168	B3	D11	IO	I	D11/GP0_11(*4)	I	On
169	A2	D12	IO	I	D12/GP0_12(*4)	I	On
170	D5	D13	IO	I	D13/GP0_13(*4)	I	On
171	D3	D14	IO	I	D14/GP0_14(*4)	I	On
172	F5	D15	IO	I	D15/GP0_15(*4)	I	On
173	F4	A0	O	I(MD3)	A0/GP0_16(*4)	L/I	Off
174	F3	A1	O	I(MD0)	A1/GP0_17(*4)	L/I	Off
175	G4	A2	O	I(MDT1)	A2/GP0_18(*4)	L/I	Off
176	H5	A3	O	I(MD2)	A3/GP0_19(*4)	L/I	Off
177	H4	A4	O	I(MD1)	A4/GP0_20(*4)	L/I	Off
178	F2	A5	O	I	A5/GP0_21(*4)	L/I	On
179	G5	A6	O	I	A6/GP0_22(*4)	L/I	On
180	F1	A7	O	I(MD4)	A7/GP0_23(*4)	L/I	Off
181	J5	A8	O	I	A8/GP0_24(*4)	L/I	On
182	G2	A9	O	I(MD5)	A9/GP0_25(*4)	L/I	Off
183	J4	A10	O	I	A10/GP0_26(*4)	L/I	On
184	H3	A11	O	I	A11/GP0_27(*4)	L/I	On
185	G3	A12	O	I	A12/GP0_28(*4)	L/I	On
186	G1	A13	O	I(MD6)	A13/GP0_29(*4)	L/I	Off
187	K5	A14	O	I	A14/GP0_30(*4)	L/I	On
188	H1	A15	O	I(MD7)	A15/GP0_31(*4)	L/I	Off
189	J2	A16	O	I	A16/GP1_0(*4)	L/I	On
190	K4	A17	O	I	A17/GP1_1(*4)	L/I	On
191	H2	A18	O	I(MDT0)	A18/GP1_2(*4)	L/I	Off
192	K3	A19	O	I(MD18)	A19/GP1_3(*4)	L/I	Off
193	K2	A20	O	I	A20/GP1_4(*4)	L/I	On
194	K1	A21	O	I	A21/GP1_5(*4)	L/I	On
195	L3	A22	O	I	A22/GP1_6(*4)	L/I	On
196	J3	A23	O	I	A23/GP1_7(*4)	L/I	On
197	J1	A24	O	I	A24/GP1_8(*4)	L/I	On
198	L2	A25	O	I	A25/GP1_9(*4)	L/I	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
199	B1	CLKOUT	O	O	CLKOUT	O	-
200	E2	CS0#	O	I	CS0#/GP1_10(*4)	H/I	On
201	M5	CS1#/A26	O	I	[CS1#/A26]/GP1_11	[H/L] (*5)/I	On
202	E1	EX_CS0#	O	I	GP1_12	I	On
203	E3	EX_CS1#	O	I	GP1_13	I	On
204	D1	EX_CS2#	O	I	GP1_14	I	On
205	D2	EX_CS3#	O	I	GP1_15	I	On
206	C1	EX_CS4#	O	I	GP1_16	I	On
207	B2	EX_CS5#	O	I	GP1_17	I	On
208	M4	BS#	O	I(MD8)	BS#/GP1_18(*4)	H/I	Off
209	M3	RD#	O	I(MD14)	RD#GP1_19(*4)	H/I	Off
210	M1	RD/WR#	O	I(MD9)	GP1_20	I	Off
211	L1	WE0#	O	I(MD19)	WE0#/ GP1_21(*4)	H/I	Off
212	L4	WE1#	O	I(MD20)	WE1#/ GP1_22(*4)	H/I	Off
213	C2	EX_WAIT0	I	I	EX_WAIT0/ GP1_23(*4)	I/I	On
214	L5	DREQ0#	I	I	GP1_24	I	On
215	M2	DACK0	O	I(MD21)	GP1_25	I	Off
216	AA18	DU0_DR0	O	I	GP2_0	I	On
217	AB18	DU0_DR1	O	I	GP2_1	I	On
218	AE19	DU0_DR2	O	I	GP2_2	I	On
219	AC18	DU0_DR3	O	I	GP2_3	I	On
220	AD19	DU0_DR4	O	I	GP2_4	I	On
221	AD17	DU0_DR5	O	I	GP2_5	I	On
222	AC17	DU0_DR6	O	I	GP2_6	I	On
223	AC19	DU0_DR7	O	I	GP2_7	I	On
224	AA17	DU0_DG0	O	I	GP2_8	I	On
225	AB16	DU0_DG1	O	I	GP2_9	I	On
226	AD18	DU0_DG2	O	I	GP2_10	I	On
227	AD16	DU0_DG3	O	I	GP2_11	I	On
228	AB17	DU0_DG4	O	I	GP2_12	I	On
229	AA16	DU0_DG5	O	I	GP2_13	I	On
230	AE16	DU0_DG6	O	I	GP2_14	I	On
231	AC16	DU0_DG7	O	I	GP2_15	I	On
232	AC14	DU0_DB0	O	I	GP2_16	I	On
233	AE17	DU0_DB1	O	I	GP2_17	I	On
234	AA15	DU0_DB2	O	I	GP2_18	I	On
235	AB15	DU0_DB3	O	I	GP2_19	I	On
236	AD14	DU0_DB4	O	I	GP2_20	I	On
237	AD15	DU0_DB5	O	I	GP2_21	I	On
238	AA14	DU0_DB6	O	I	GP2_22	I	On
239	AC15	DU0_DB7	O	I	GP2_23	I	On
240	AE15	DU0_DOTCLKIN	I	I	GP2_24	I	On
241	AE14	DU0_DOTCLKOUT0	O	I	GP2_25	I	On
242	AE13	DU0_DOTCLKOUT1	O	I	GP2_26	I	On
243	AD13	DU0_EXHSYNC/DU0_HSYNC	IO	I(MD11)	GP2_27	I	Off
244	AB14	DU0_EXVSYNC/DU0_VSYNC	IO	I(MD12)	GP2_28	I	Off
245	AC13	DU0_EXODDF/DU0_ODDF/DISP/CDE	IO	I	GP2_29	I	On
246	AE18	DU0_DISP	O	I(MD10)	GP2_30	I	Off
247	AB13	DU0_CDE	O	I(MD13)	GP2_31	I	Off
248	AB1	VI0_CLK	I	I	GP3_0	I	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
249	AA4	VI0_DATA0/VI0_B0	I	I	GP3_1	I	On
250	AB3	VI0_DATA1/VI0_B1	I	I	GP3_2	I	On
251	AA3	VI0_DATA2/VI0_B2	I	I	GP3_3	I	On
252	AB2	VI0_DATA3/VI0_B3	I	I	GP3_4	I	On
253	Y3	VI0_DATA4/VI0_B4	I	I	GP3_5	I	On
254	W3	VI0_DATA5/VI0_B5	I	I	GP3_6	I	On
255	Y2	VI0_DATA6/VI0_B6	I	I	GP3_7	I	On
256	AA2	VI0_DATA7/VI0_B7	I	I	GP3_8	I	On
257	AA1	VI0_CLKENB	I	I	GP3_9	I	On
258	W2	VI0_FIELD	I	I	GP3_10	I	On
259	Y1	VI0_HSYNC#	I	I	GP3_11	I	On
260	W1	VI0_VSYNC#	I	I	GP3_12	I	On
261	T5	ETH_MDIO	IO	I	GP3_13	I	On
262	V4	ETH_CRS_DV	I	I	GP3_14	I	On
263	U5	ETH_RX_ER	I	I	GP3_15	I	On
264	V3	ETH_RXD0	I	I	GP3_16	I	On
265	U4	ETH_RXD1	I	I	GP3_17	I	On
266	V5	ETH_LINK	I	I	GP3_18	I	On
267	V1	ETH_REF_CLK	I	I	GP3_19	I	On
268	V2	ETH_TXD1	O	I	GP3_20	I	On
269	U3	ETH_TX_EN	O	I	GP3_21	I	On
270	W4	ETH_MAGIC	O	I	GP3_22	I	On
271	U2	ETH_TXD0	O	I	GP3_23	I	On
272	W5	ETH_MDC	O	I	GP3_24	I	On
273	U1	HSCIF0_HRX	I	I	GP3_25	I	On
274	T4	HSCIF0_HTX	O	I	GP3_26	I	On
275	T3	HSCIF0_HCTS#	IO	I	GP3_27	I	On
276	T2	HSCIF0_HRTS#	IO	I	GP3_28	I	On
277	T1	HSCIF0_HSCK	IO	I	GP3_29	I	On
278	Y5	I2C0_SCL	IO	I	GP3_30	I	On
279	Y4	I2C0_SDA	IO	I	GP3_31	I	On
280	Y24	I2C1_SCL	IO	I	GP4_0	I	On
281	Y25	I2C1_SDA	IO	I	GP4_1	I	On
282	W24	MSIOF0_RXD	I	I	GP4_2	I	On
283	W23	MSIOF0_TXD	O	I	GP4_3	I	On
284	AA25	MSIOF0_SCK	IO	I	GP4_4	I	On
285	AB25	MSIOF0_SYNC	IO	I	GP4_5	I	On
286	Y22	MSIOF0_SS1	O	I	GP4_6	I	On
287	W22	MSIOF0_SS2	O	I	GP4_7	I	On
288	AB23	HSCIF1_HRX	I	I	GP4_8	I	On
289	AA23	HSCIF1_HTX	O	I	GP4_9	I	On
290	AA24	HSCIF1_HSCK	IO	I	GP4_10	I	On
291	Y23	HSCIF1_HCTS#	IO	I	GP4_11	I	On
292	AB24	HSCIF1_HRTS#	IO	I	GP4_12	I	On
293	AC25	SCIF1_SCK	IO	I	GP4_13	I	On
294	AD25	SCIF1_RXD	I	I	GP4_14	I	On
295	AC24	SCIF1_TXD	O	I	GP4_15	I	On
296	AD23	SCIF2_RXD	I	I	GP4_16	I	On
297	AE23	SCIF2_TXD	O	I	GP4_17	I	On
298	AE24	SCIF2_SCK	IO	I	GP4_18	I	On

No.	Pin No.	Pin Name (Function 1)	I/O	During POR	Default Pin Function	Default State	Default Pull-up
299	AA22	SCIF3_SCK	IO	I	GP4_19	I	On
300	AC22	SCIF3_RXD	I	I	GP4_20	I	On
301	AC21	SCIF3_TXD	O	I	GP4_21	I	On
302	AD21	I2C2_SCL	IO	I	GP4_22	I	On
303	AC20	I2C2_SDA	IO	I	GP4_23	I	On
304	AE22	SSI_SCK5	IO	I	GP4_24	I	On
305	AB20	SSI_WS5	IO	I	GP4_25	I	On
306	AA20	SSI_SDATA5	IO	I	GP4_26	I	On
307	AE20	SSI_SCK6	IO	I	GP4_27	I	On
308	AD20	SSI_WS6	IO	I	GP4_28	I	On
309	AE21	SSI_SDATA6	IO	I	GP4_29	I	On
310	AB19	SSI_SCK78	IO	I	GP4_30	I	On
311	AA19	SSI_WS78	IO	I	GP4_31	I	On
312	AB7	SSI_SDATA7	IO	I	GP5_0	I	On
313	AE5	SSI_SCK0129	IO	I	GP5_1	I	On
314	AA7	SSI_WS0129	IO	I	GP5_2	I	On
315	AA6	SSI_SDATA0	IO	I	GP5_3	I	On
316	AD6	SSI_SCK34	IO	I	GP5_4	I	On
317	AB6	SSI_WS34	IO	I	GP5_5	I	On
318	AD5	SSI_SDATA3	IO	I	GP5_6	I	On
319	AD22	SSI_SCK4	IO	I	GP5_7	I	-
320	AB21	SSI_WS4	IO	I	GP5_8	I	-
321	Y21	SSI_SDATA4	IO	I	GP5_9	I	-
322	AD24	MLB_REF	IO	IO	Reserved	IO	-
323	W20	VSS_MLBPLL	-	P	-	P	-
324	V21	VDD_MLBPLL	-	P	-	P	-
325	AC6	SSI_SDATA8	IO	I	GP5_10	I	On
326	AE6	SSI_SCK1	IO	I	GP5_11	I	On
327	AB5	SSI_WS1	IO	I	GP5_12	I	On
328	AC5	SSI_SDATA1	IO	I	GP5_13	I	On
329	AE4	SSI_SCK2	IO	I	GP5_14	I	On
330	AD4	SSI_WS2	IO	I	GP5_15	I	On
331	AC4	SSI_SDATA2	IO	I	GP5_16	I	On
332	AE3	SSI_SCK9	IO	I	GP5_17	I	On
333	AD3	SSI_WS9	IO	I	GP5_18	I	On
334	AD2	SSI_SDATA9	IO	I	GP5_19	I	On
335	AD1	AUDIO_CLKA	I	I	GP5_20	I	On
336	AE2	AUDIO_CLKB	I	I	GP5_21	I	On
337	AC1	AUDIO_CLKC	I	I	GP5_22	I	On
338	AC2	AUDIO_CLKOUT	O	I	GP5_23	I	On
339	W21	IIC1_SCL	IO	Z	IIC1_SCL	Z	-
340	V22	IIC1_SDA	IO	Z	IIC1_SDA	Z	-

Notes: 1. No.47, 48, 61, 62, 74, 75, 88 and 89 (M0DQSx and M0DQSx#) pin states during POR and default state:
The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQSx pin and high-level for the M0DQSx# pin respectively.

2. No.137 to 142 and 146 to 151 Default pin function and pin state:
Depends on MD[21:20], MD[12:10], and MDT[1:0] settings.
"I" is in function mode (GPIO); "Z" is in debug mode.

3. No.138 to 142 and 147 to 151 Default pull-up:
"-" is in debugging operation only; "Off" is in other than debugging operation.

4. No.157 to 198, 200, 201, 208, 209, and 211 to 213 Default pin function:
   MD[3:1] = 000: LBSC (D[15:0], A[25:0], CS0#, CS1#/A26, BS#, RD#, WE[1:0]#, and EX_WAIT0)
   MD[3:1] ≠ 000: GPIO (GP0_[31:0], GP1_[11:0], [19:18], [23:21])
5. No.201 CS1#/A26 Default state:
   MD4 = 0: (area 0 64-Mbyte mode): high output
   MD4 = 1: (area 0 128-Mbyte mode): low output

4.3 Handling of Unused Pins

Table 4.3 shows a handling of unused pins of the RZ/G1E.

"Unused pin" means all modules that are multiplexed to the pin should be disable and unused in this section. For handling of some unused pin which belongs to the enable module should be handled following the notification of the module manual. Unless otherwise specified in the module manual, follow the Table 4.3 for handling of unused pins.

[Legend]

No.: Serial number, Pin No.: BGA package ball grid number, Pin Name: Pin name of function 1 in pin multiplex table, Default State: Pin state of default pin function (function 1, GPIO or DBG).

Mode Pin: Mode pin assigned.

Boot: These pins will be used in boot operation (LBSC area 0 or QSPI).

Default pull-up: Internal pull-up control function is available or not from a power-on reset and its pull-up state.

"On": Pull-up control function is available and default state is pulled-up.

(No.110, ACK pin is available internal pull-down function.)

"Off": Pull-up control function is available and default state is not pulled-up.

"-": Pull-up control function is not available.

For details of pull-up control function, refer to PUPR0 through PUPR12 registers in section 5, Pin Function Controller (PFC).

Notes: 1. All power supply pins and ground pins including VCCQ, VCCQ18, VDD, VDDQ_M0, VDDQ_M0BKUP and VSS pins which are not described in Table 4.3 must be used.

2. All mode pins (MD[21:18],[14:0] and MDT[1:0]) must be used during power-on reset. For details of mode pins setting, refer to section 3.3, Mode Pin Settings.

3. Boot related pins (LBSC or QSPI) should be used during boot operation. For details of QSPI boot, refer to section 18, Booting.

Table 4.3 Handling of Unused Pins

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
1	D15	M0CKE0	O(L)	-	-	-	Open
2	E11	M0CKE1	O(L)	-	-	-	Open
3	D14	M0VREFCA	P	-	-	-	Must be used
4	E7	M0BKPRST#	I	-	-	-	Pulled-up to VDDQ_M0BKUP or pulled-down to VSS
5	D12	M0RESET#	H to L	-	-	-	Open
6	A15	M0CK0	O	-	-	-	Open
7	A14	M0CK0#	O	-	-	-	Open
8	C11	M0CK1	O	-	-	-	Open
9	C10	M0CK1#	O	-	-	-	Open
10	C15	M0CS0#	H	-	-	-	Open
11	E10	M0CS1#	H	-	-	-	Open
12	B16	M0ODT0	L	-	-	-	Open
13	D11	M0ODT1	L	-	-	-	Open
14	D9	M0ZQ	IO	-	-	-	Must be used
15	E14	M0WE#	H	-	-	-	Open
16	D16	M0RAS#	H	-	-	-	Open
17	E13	M0CAS#	H	-	-	-	Open
18	B9	M0A0	L	-	-	-	Open
19	B12	M0A1	L	-	-	-	Open
20	A11	M0A2	L	-	-	-	Open
21	B10	M0A3	L	-	-	-	Open
22	B13	M0A4	L	-	-	-	Open
23	B8	M0A5	L	-	-	-	Open
24	A7	M0A6	L	-	-	-	Open
25	B14	M0A7	L	-	-	-	Open
26	D8	M0A8	L	-	-	-	Open
27	B11	M0A9	L	-	-	-	Open
28	A8	M0A10	L	-	-	-	Open
29	A9	M0A11	L	-	-	-	Open
30	A6	M0A12	L	-	-	-	Open
31	B7	M0A13	L	-	-	-	Open
32	D7	M0A14	L	-	-	-	Open
33	A12	M0A15	L	-	-	-	Open
34	E12	M0BA0	L	-	-	-	Open
35	A10	M0BA1	L	-	-	-	Open
36	D13	M0BA2	L	-	-	-	Open
37	F12	VDDQ_M0APLL	P	-	-	-	Must be used
38	F13	VSSQ_M0APLL	P	-	-	-	Must be used
39	E20	M0DQ0	Z	-	-	-	Open
40	D21	M0DQ1	Z	-	-	-	Open
41	A24	M0DQ2	Z	-	-	-	Open
42	B22	M0DQ3	Z	-	-	-	Open
43	C20	M0DQ4	Z	-	-	-	Open
44	B23	M0DQ5	Z	-	-	-	Open
45	A23	M0DQ6	Z	-	-	-	Open
46	C22	M0DQ7	Z	-	-	-	Open
47	A21	M0DQS0	Z(*1)	-	-	-	Open
48	A20	M0DQS0#	Z(*1)	-	-	-	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
49	C21	M0DM0	Z	-	-	-	Open
50	F16	VDDQ_M0DPLL0	P	-	-	-	Must be used
51	F15	VSSQ_M0DPLL0	P	-	-	-	Must be used
52	C14	M0VREFDQ0	P	-	-	-	Must be used
53	B17	M0DQ8	Z	-	-	-	Open
54	D17	M0DQ9	Z	-	-	-	Open
55	B19	M0DQ10	Z	-	-	-	Open
56	B20	M0DQ11	Z	-	-	-	Open
57	D19	M0DQ12	Z	-	-	-	Open
58	E19	M0DQ13	Z	-	-	-	Open
59	B18	M0DQ14	Z	-	-	-	Open
60	E18	M0DQ15	Z	-	-	-	Open
61	A18	M0DQS1	Z(*1)	-	-	-	Open
62	A17	M0DQS1#	Z(*1)	-	-	-	Open
63	D18	M0DM1	Z	-	-	-	Open
64	E16	VDDQ_M0DPLL1	P	-	-	-	Must be used
65	E15	VSSQ_M0DPLL1	P	-	-	-	Must be used
66	G24	M0DQ16	Z	-	-	-	Open
67	E22	M0DQ17	Z	-	-	-	Open
68	E24	M0DQ18	Z	-	-	-	Open
69	C25	M0DQ19	Z	-	-	-	Open
70	F24	M0DQ20	Z	-	-	-	Open
71	D24	M0DQ21	Z	-	-	-	Open
72	B25	M0DQ22	Z	-	-	-	Open
73	C24	M0DQ23	Z	-	-	-	Open
74	F25	M0DQS2	Z(*1)	-	-	-	Open
75	E25	M0DQS2#	Z(*1)	-	-	-	Open
76	F22	M0DM2	Z	-	-	-	Open
77	J21	VDDQ_M0DPLL2	P	-	-	-	Must be used
78	H21	VSSQ_M0DPLL2	P	-	-	-	Must be used
79	G23	M0VREFDQ1	P	-	-	-	Must be used
80	J23	M0DQ24	Z	-	-	-	Open
81	K22	M0DQ25	Z	-	-	-	Open
82	H22	M0DQ26	Z	-	-	-	Open
83	L22	M0DQ27	Z	-	-	-	Open
84	J24	M0DQ28	Z	-	-	-	Open
85	L24	M0DQ29	Z	-	-	-	Open
86	K24	M0DQ30	Z	-	-	-	Open
87	L25	M0DQ31	Z	-	-	-	Open
88	H25	M0DQS3	Z(*1)	-	-	-	Open
89	J25	M0DQS3#	Z(*1)	-	-	-	Open
90	J22	M0DM3	Z	-	-	-	Open
91	J20	VDDQ_M0DPLL3	P	-	-	-	Must be used
92	H20	VSSQ_M0DPLL3	P	-	-	-	Must be used
93	C7	VDDQ_M0BKUP	P	-	-	-	Must be used
94	V25	EXTAL	I	-	-	-	Must be used
95	V24	XTAL	O	-	-	-	Open
96	E8	VDD_CPGPLL0	P	-	-	-	Must be used
97	E9	VSS_CPGPLL0	P	-	-	-	Must be used
98	K15/L15	VDD_CPGPLL1	P	-	-	-	Must be used

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
99	K16/L16	VSS_CPGPLL1	P	-	-	-	Must be used
100	K12/L12	VDD_CPGPLL3	P	-	-	-	Must be used
101	K11/L11	VSS_CPGPLL3	P	-	-	-	Must be used
102	V23	PRESET#	I	-	-	-	Must be used
103	B6	PRESETOUT#	L to H	-	-	-	Open
104	R21	BSMODE	I	-	-	-	Must be used
105	N21	TRST#	I	-	-	On	Pulled-down to VSS
106	N22	TCK	I	-	-	On	Open
107	P21	TMS	I	-	-	On	Open
108	R22	TDI	I	-	-	On	Open
109	P22	TDO	Z	-	-	-	Open
110	U23	ACK	I	-	-	On(pulldown)	Open
111	T25	USB_EXTAL	I	-	-	-	Pulled-down to VSS
112	T24	USB_XTAL	O	-	-	-	Open
113	P20	VD331	P	-	-	-	Must be used
114	R20	VD181	P	-	-	-	Must be used
115	P23	AVDD	P	-	-	-	Must be used
116	M20	AVSS	P	-	-	-	Must be used
117	P24	USB0_DP	I	-	-	-	Open
118	P25	USB0_DM	I	-	-	-	Open
119	M25	USB0_RREF	P	-	-	-	Must be used
120	U21	USB0_PWEN	L	-	-	-	Open
121	U22	USB0_OVC	I	-	-	-	Pulled-down to VSS
122	N24	USB1_DP	I	-	-	-	Open
123	N25	USB1_DM	I	-	-	-	Open
124	M24	USB1_RREF	P	-	-	-	Must be used
125	T21	USB1_PWEN	L	-	-	-	Open
126	T22	USB1_OVC	I	-	-	-	Pulled-down to VSS
127	R23	NMI	I	-	-	-	Should be used (recommendable)
128	AE12	SD0_CLK	I	-	-	-	Pulled-up to VCCQ_SD0 or pulled-down to VSS
129	AD12	SD0_CMD	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
130	AC11	SD0_DATA0	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
131	AD11	SD0_DATA1	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
132	AE11	SD0_DATA2	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
133	AA12	SD0_DATA3	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
134	AB12	SD0_CD	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
135	AA13	SD0_WP	I	-	-	Off	Pulled-up to VCCQ_SD0 or pulled-down to VSS
136	AC12	VCCQ_SD0	P	-	-	-	Must be used
137	AE8	SD1_CLK	I/Z(*2)	-	-	-	Pulled-up to VCCQ_SD1 or pulled-down to VSS
138	AA8	SD1_CMD	I	-	-	Off/-(*3)	Pulled-up to VCCQ_SD1 or pulled-down to VSS
139	AD7	SD1_DATA0	I	-	-	Off/-(*3)	Pulled-up to VCCQ_SD1 or pulled-down to VSS
140	AE7	SD1_DATA1	I	-	-	Off/-(*3)	Pulled-up to VCCQ_SD1 or pulled-down to VSS
141	AB8	SD1_DATA2	I	-	-	Off/-(*3)	Pulled-up to VCCQ_SD1 or pulled-down to VSS
142	AC8	SD1_DATA3	I	-	-	Off/-(*3)	Pulled-up to VCCQ_SD1 or pulled-down to VSS
143	AD8	SD1_CD	I	-	-	Off	Pulled-up to VCCQ_SD1 or pulled-down to VSS
144	AE9	SD1_WP	I	-	-	Off	Pulled-up to VCCQ_SD1 or pulled-down to VSS
145	AC7	VCCQ_SD1	P	-	-	-	Must be used
146	AE10	MMC_CLK	I/Z(*2)	-	-	-	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
147	AD9	MMC_CMD	I	-	-	Off/-(*3)	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
148	AA9	MMC_D0	I	-	-	Off/-(*3)	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
149	AA11	MMC_D1	I	-	-	Off/-(*3)	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
150	AC9	MMC_D2	I	-	-	Off/-(*3)	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
151	AA10	MMC_D3	I	-	-	Off/-(*3)	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
152	AB10	MMC_D4	I	-	-	Off	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
153	AD10	MMC_D5	I	-	-	Off	Pulled-up to VCCQ_MMC_SD2 or pulled-down to VSS
154	AB9	MMC_D6	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
155	AB11	MMC_D7	I	-	-	Off	Pulled-up to VCCQ or pulled-down to VSS
156	AC10	VCCQ_MMC_SD2	P	-	-	-	Must be used
157	D6	D0	I	-	Area 0	On	Open
158	E6	D1	I	-	Area 0	On	Open
159	A5	D2	I	-	Area 0	On	Open
160	C6	D3	I	-	Area 0	On	Open
161	A4	D4	I	-	Area 0	On	Open
162	C5	D5	I	-	Area 0	On	Open
163	B4	D6	I	-	Area 0	On	Open
164	B5	D7	I	-	Area 0	On	Open
165	C4	D8	I	-	Area 0	On	Open
166	A3	D9	I	-	Area 0	On	Open
167	E4	D10	I	-	Area 0	On	Open
168	B3	D11	I	-	Area 0	On	Open
169	A2	D12	I	-	Area 0	On	Open
170	D5	D13	I	-	Area 0	On	Open
171	D3	D14	I	-	Area 0	On	Open
172	F5	D15	I	-	Area 0	On	Open
173	F4	A0	L/I	MD3	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
174	F3	A1	L/I	MD0	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
175	G4	A2	L/I	MDT1	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
176	H5	A3	L/I	MD2	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
177	H4	A4	L/I	MD1	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
178	F2	A5	L/I	-	Area 0	On	Open
179	G5	A6	L/I	-	Area 0	On	Open
180	F1	A7	L/I	MD4	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
181	J5	A8	L/I	-	Area 0	On	Open
182	G2	A9	L/I	MD5	Area 0	Off	Pulled-up to VCCQ
183	J4	A10	L/I	-	Area 0	On	Open
184	H3	A11	L/I	-	Area 0	On	Open
185	G3	A12	L/I	-	Area 0	On	Open
186	G1	A13	L/I	MD6	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
187	K5	A14	L/I	-	Area 0	On	Open
188	H1	A15	L/I	MD7	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
189	J2	A16	L/I	-	Area 0	On	Open
190	K4	A17	L/I	-	Area 0	On	Open
191	H2	A18	L/I	MDT0	-	Off	Pulled-up to VCCQ or pulled-down to VSS
192	K3	A19	L/I	MD18	-	Off	Pulled-down to VSS
193	K2	A20	L/I	-	QSPI	On	Open
194	K1	A21	L/I	-	QSPI	On	Open
195	L3	A22	L/I	-	QSPI	On	Open
196	J3	A23	L/I	-	QSPI	On	Open
197	J1	A24	L/I	-	QSPI	On	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
198	L2	A25	L/I	-	QSPI	On	Open
199	B1	CLKOUT	O	-	Area 0	-	Open
200	E2	CS0#	H/I	-	Area 0	On	Open
201	M5	[CS1#/A26]	[H or L] (*4)/I	-	Area 0	On	Open
202	E1	EX_CS0#	I	-	-	On	Open
203	E3	EX_CS1#	I	-	-	On	Open
204	D1	EX_CS2#	I	-	-	On	Open
205	D2	EX_CS3#	I	-	-	On	Open
206	C1	EX_CS4#	I	-	-	On	Open
207	B2	EX_CS5#	I	-	-	On	Open
208	M4	BS#	H/I	MD8	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
209	M3	RD#	H/I	MD14	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
210	M1	RD/WR#	I	MD9	-	Off	Pulled-up to VCCQ or pulled-down to VSS
211	L1	WE0#	H/I	MD19	Area 0	Off	Pulled-up to VCCQ
212	L4	WE1#	H/I	MD20	Area 0	Off	Pulled-up to VCCQ or pulled-down to VSS
213	C2	EX_WAIT0	I/I	-	Area 0	On	Open
214	L5	DREQ0#	I	-	-	On	Open
215	M2	DACK0	I	MD21	-	Off	Pulled-up to VCCQ or pulled-down to VSS
216	AA18	DU0_DR0	I	-	-	On	Open
217	AB18	DU0_DR1	I	-	-	On	Open
218	AE19	DU0_DR2	I	-	-	On	Open
219	AC18	DU0_DR3	I	-	-	On	Open
220	AD19	DU0_DR4	I	-	-	On	Open
221	AD17	DU0_DR5	I	-	-	On	Open
222	AC17	DU0_DR6	I	-	-	On	Open
223	AC19	DU0_DR7	I	-	-	On	Open
224	AA17	DU0_DG0	I	-	-	On	Open
225	AB16	DU0_DG1	I	-	-	On	Open
226	AD18	DU0_DG2	I	-	-	On	Open
227	AD16	DU0_DG3	I	-	-	On	Open
228	AB17	DU0_DG4	I	-	-	On	Open
229	AA16	DU0_DG5	I	-	-	On	Open
230	AE16	DU0_DG6	I	-	-	On	Open
231	AC16	DU0_DG7	I	-	-	On	Open
232	AC14	DU0_DB0	I	-	-	On	Open
233	AE17	DU0_DB1	I	-	-	On	Open
234	AA15	DU0_DB2	I	-	-	On	Open
235	AB15	DU0_DB3	I	-	-	On	Open
236	AD14	DU0_DB4	I	-	-	On	Open
237	AD15	DU0_DB5	I	-	-	On	Open
238	AA14	DU0_DB6	I	-	-	On	Open
239	AC15	DU0_DB7	I	-	-	On	Open
240	AE15	DU0_DOTCLKIN	I	-	-	On	Open
241	AE14	DU0_DOTCLKOUT0	I	-	-	On	Open
242	AE13	DU0_DOTCLKOUT1	I	-	-	On	Open
243	AD13	DU0_EXHSYNC/DU0_HSYNC	I	MD11	-	Off	Pulled-up to VCCQ or pulled-down to VSS
244	AB14	DU0_EXVSYNC/DU0_VSYNC	I	MD12	-	Off	Pulled-up to VCCQ or pulled-down to VSS

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
245	AC13	DU0_EXODDF/DU0_ODDF/DISP/CDE	I	-	-	On	Open
246	AE18	DU0_DISP	I	MD10	-	Off	Pulled-up to VCCQ or pulled-down to VSS
247	AB13	DU0_CDE	I	MD13	-	Off	Pulled-up to VCCQ or pulled-down to VSS
248	AB1	VI0_CLK	I	-	-	On	Open
249	AA4	VI0_DATA0/VI0_B0	I	-	-	On	Open
250	AB3	VI0_DATA1/VI0_B1	I	-	-	On	Open
251	AA3	VI0_DATA2/VI0_B2	I	-	-	On	Open
252	AB2	VI0_DATA3/VI0_B3	I	-	-	On	Open
253	Y3	VI0_DATA4/VI0_B4	I	-	-	On	Open
254	W3	VI0_DATA5/VI0_B5	I	-	-	On	Open
255	Y2	VI0_DATA6/VI0_B6	I	-	-	On	Open
256	AA2	VI0_DATA7/VI0_B7	I	-	-	On	Open
257	AA1	VI0_CLKENB	I	-	-	On	Open
258	W2	VI0_FIELD	I	-	-	On	Open
259	Y1	VI0_HSYNC#	I	-	-	On	Open
260	W1	VI0_VSYNC#	I	-	-	On	Open
261	T5	ETH_MDIO	I	-	-	On	Open
262	V4	ETH_CRS_DV	I	-	-	On	Open
263	U5	ETH_RX_ER	I	-	-	On	Open
264	V3	ETH_RXD0	I	-	-	On	Open
265	U4	ETH_RXD1	I	-	-	On	Open
266	V5	ETH_LINK	I	-	-	On	Open
267	V1	ETH_REF_CLK	I	-	-	On	Open
268	V2	ETH_TXD1	I	-	-	On	Open
269	U3	ETH_TX_EN	I	-	-	On	Open
270	W4	ETH_MAGIC	I	-	-	On	Open
271	U2	ETH_TXD0	I	-	-	On	Open
272	W5	ETH_MDC	I	-	-	On	Open
273	U1	HSCIF0_HRX	I	-	-	On	Open
274	T4	HSCIF0_HTX	I	-	-	On	Open
275	T3	HSCIF0_HCTS#	I	-	-	On	Open
276	T2	HSCIF0_HRTS#	I	-	-	On	Open
277	T1	HSCIF0_HSCK	I	-	-	On	Open
278	Y5	I2C0_SCL	I	-	-	On	Open
279	Y4	I2C0_SDA	I	-	-	On	Open
280	Y24	I2C1_SCL	I	-	-	On	Open
281	Y25	I2C1_SDA	I	-	-	On	Open
282	W24	MSIOF0_RXD	I	-	-	On	Open
283	W23	MSIOF0_TXD	I	-	-	On	Open
284	AA25	MSIOF0_SCK	I	-	-	On	Open
285	AB25	MSIOF0_SYNC	I	-	-	On	Open
286	Y22	MSIOF0_SS1	I	-	-	On	Open
287	W22	MSIOF0_SS2	I	-	-	On	Open
288	AB23	HSCIF1_HRX	I	-	-	On	Open
289	AA23	HSCIF1_HTX	I	-	-	On	Open
290	AA24	HSCIF1_HSCK	I	-	-	On	Open
291	Y23	HSCIF1_HCTS#	I	-	-	On	Open
292	AB24	HSCIF1_HRTS#	I	-	-	On	Open
293	AC25	SCIF1_SCK	I	-	-	On	Open

No.	Pin No.	Pin Name (Function 1)	Default State	Mode Pin	Boot	Default Pull-up	Pin Handling when not in Use
294	AD25	SCIF1_RXD	I	-	-	On	Open
295	AC24	SCIF1_TXD	I	-	-	On	Open
296	AD23	SCIF2_RXD	I	-	-	On	Open
297	AE23	SCIF2_TXD	I	-	-	On	Open
298	AE24	SCIF2_SCK	I	-	-	On	Open
299	AA22	SCIF3_SCK	I	-	-	On	Open
300	AC22	SCIF3_RXD	I	-	-	On	Open
301	AC21	SCIF3_TXD	I	-	-	On	Open
302	AD21	I2C2_SCL	I	-	-	On	Open
303	AC20	I2C2_SDA	I	-	-	On	Open
304	AE22	SSI_SCK5	I	-	-	On	Open
305	AB20	SSI_WS5	I	-	-	On	Open
306	AA20	SSI_SDATA5	I	-	-	On	Open
307	AE20	SSI_SCK6	I	-	-	On	Open
308	AD20	SSI_WS6	I	-	-	On	Open
309	AE21	SSI_SDATA6	I	-	-	On	Open
310	AB19	SSI_SCK78	I	-	-	On	Open
311	AA19	SSI_WS78	I	-	-	On	Open
312	AB7	SSI_SDATA7	I	-	-	On	Open
313	AE5	SSI_SCK0129	I	-	-	On	Open
314	AA7	SSI_WS0129	I	-	-	On	Open
315	AA6	SSI_SDATA0	I	-	-	On	Open
316	AD6	SSI_SCK34	I	-	-	On	Open
317	AB6	SSI_WS34	I	-	-	On	Open
318	AD5	SSI_SDATA3	I	-	-	On	Open
319	AD22	SSI_SCK4	I	-	-	-	Pulled-up to VCCQ or pulled-down to VSS
320	AB21	SSI_WS4	I	-	-	-	Pulled-up to VCCQ or pulled-down to VSS
321	Y21	SSI_SDATA4	I	-	-	-	Pulled-up to VCCQ or pulled-down to VSS
322	AD24	MLB_REF	IO	-	-	-	Open
323	W20	VSS_MLBPLL	P	-	-	-	-
324	V21	VDD_MLBPLL	P	-	-	-	-
325	AC6	SSI_SDATA8	I	-	-	On	Open
326	AE6	SSI_SCK1	I	-	-	On	Open
327	AB5	SSI_WS1	I	-	-	On	Open
328	AC5	SSI_SDATA1	I	-	-	On	Open
329	AE4	SSI_SCK2	I	-	-	On	Open
330	AD4	SSI_WS2	I	-	-	On	Open
331	AC4	SSI_SDATA2	I	-	-	On	Open
332	AE3	SSI_SCK9	I	-	-	On	Open
333	AD3	SSI_WS9	I	-	-	On	Open
334	AD2	SSI_SDATA9	I	-	-	On	Open
335	AD1	AUDIO_CLKA	I	-	-	On	Open
336	AE2	AUDIO_CLKB	I	-	-	On	Open
337	AC1	AUDIO_CLKC	I	-	-	On	Open
338	AC2	AUDIO_CLKOUT	I	-	-	On	Open
339	W21	IIC1_SCL	Z	-	-	-	Pulled-up to VCCQ18
340	V22	IIC1_SDA	Z	-	-	-	Pulled-up to VCCQ18

Notes: 1. No.47, 48, 61, 62, 74, 75, 88 and 89 (M0DQSx and M0DQSx#) pin states during POR and default state:
The drivers output states are both high-impedance (Z), and the internal circuit controls pin levels as low-level for the M0DQSx pin and high-level for the M0DQSx# pin respectively.

2. No.137 to 142 and 146 to 151 Default pin function and pin state:
Depends on MD[21:20], MD[12:10], and MDT[1:0] settings.
"I" is in function mode (GPIO); "Z" is in debug mode.

3. No.138 to 142 and 147 to 151 Default pull-up:
"-" is in debugging operation only; "Off" is in other than debugging operation.

4. No.201 CS1#/A26 Default state:
MD4 = 0: (area 0 64-Mbyte mode): high output
MD4 = 1: (area 0 128-Mbyte mode): low output

5. Pin Function Controller (PFC)

5.1 Overview

The pin function controller (PFC) is a module that consists of registers for selecting the function of the multiplexed pins and controlling the pull-up resistor on each LSI pin.

Notes: 1. Some functions are optional or internal.
2. Pin function name that has two or more functions is indicated by using "_" instead of "/".

5.1.1 Features

- Register access through the APB bus interface
- Setting multiplexed pin functions for LSI pins

  Function of the RZ/G1E pin selectable by setting the registers in the PFC module

  (The function of the LSI pin can be selected by the GPIO/peripheral function select registers 0 to 6 (GPSR0 to GPSR6) and peripheral function select registers 0 to 13 (IPSR0 to IPSR13) in the PFC module. For details, see sections 5.3.2, GPIO/Peripheral Function Select Register 0 (GPSR0) through 5.3.22, Peripheral Function Select Register 13 (IPSR13).)
- Module selection

  Enable and disable the functions of RZ/G1E LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module.

  (Selection is handled by the module select register (MOD_SEL), module select register 2 (MOD_SEL2), and module select register 3 (MOD_SEL3). For details, see sections 5.3.23, Module Select Register (MOD_SEL), through 5.3.25, Module Select Register 3 (MOD_SEL3).
- Pull-up control for each LSI pin.

  On/off of the pull-up or pull-down resistors on each LSI pin can be controlled by setting the registers in the PFC module.

  (The pull-up, pull-down resistors on each LSI pin can be turned on or off individually by setting the LSI pin pull-up/down control registers 0 to 6 (PUPR0 to PUPR6) in the PFC module. For details, see sections 5.3.26, LSI Pin Pull-Up Control register 0 (PUPR0) through 5.3.32, LSI Pin Pull-Up Control Register 6 (PUPR6).)
- Control of IO functions, including MMC, IIC, LBSC, VI, SCIF, SRU, IRQ, DU, Ethernet and ADG.

  SDIO functions, including the driving ability, POC of pins, can be controlled by setting registers of the PFC module. For details, see sections 5.3.33 to section 5.3.37 (IOCTRL0 to IOCTRL3 and IOCRTL7).

5.2 Register Configuration

All the registers in the PFC are mapped into the APB bus space. Table 5.1 shows the configuration of the registers provided in the PFC. Details on each register in the PFC are given in sections 5.2.1 to 5.3.48.

Table 5.1 Configuration of Registers in PFC

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
LSI Multiplexed Pin Setting Mask Register	PMMR	R/W	H'0000 0000	H'E606 0000	32	—
GPIO/peripheral function select register 0	GPSR0	R/W	H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	H'E606 0004	32	—
GPIO/peripheral function select register 1	GPSR1	R/W	H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	H'E606 0008	32	—
GPIO/peripheral function select register 2	GPSR2	R/W	H'0000 0000	H'E606 000C	32	—
GPIO/peripheral function select register 3	GPSR3	R/W	H'0000 0000	H'E606 0010	32	—
GPIO/peripheral function select register 4	GPSR4	R/W	H'0000 0000	H'E606 0014	32	—
GPIO/peripheral function select register 5	GPSR5	R/W	H'0F00 0000	H'E606 0018	32	—
GPIO/peripheral function select register 6	GPSR6	R/W	H'0000 0000	H'E606 001C	32	—
Peripheral function select register 0	IPSR0	R/W	H'0000 0000	H'E606 0020	32	—
Peripheral function select register 1	IPSR1	R/W	H'0000 0000	H'E606 0024	32	—
Peripheral function select register 2	IPSR2	R/W	H'0000 0000	H'E606 0028	32	—
Peripheral function select register 3	IPSR3	R/W	H'0000 0000	H'E606 002C	32	—
Peripheral function select register 4	IPSR4	R/W	H'0000 0000	H'E606 0030	32	—
Peripheral function select register 5	IPSR5	R/W	H'0000 0000	H'E606 0034	32	—
Peripheral function select register 6	IPSR6	R/W	H'0000 0000	H'E606 0038	32	—
Peripheral function select register 7	IPSR7	R/W	H'0000 0000	H'E606 003C	32	—
Peripheral function select register 8	IPSR8	R/W	H'0000 0000	H'E606 0040	32	—
Peripheral function select register 9	IPSR9	R/W	H'0000 0000	H'E606 0044	32	—

Name	Abbr.	R/W	Initial Value	Address	Access Size	Condition
Peripheral function select register 10	IPSR10	R/W	H'0000 0000	H'E606 0048	32	—
Peripheral function select register 11	IPSR11	R/W	H'0000 0000	H'E606 004C	32	—
Peripheral function select register 12	IPSR12	R/W	H'0000 0000	H'E606 0050	32	—
Peripheral function select register 13	IPSR13	R/W	H'0000 0000	H'E606 0054	32	—
Module select register	MOD_SEL	R/W	H'0000 0000	H'E606 0090	32	—
Module select register 2	MOD_SEL2	R/W	H'0000 0000	H'E606 0094	32	—
Module select register 3	MOD_SEL3	R/W	H'0000 0000	H'E606 0098	32	—
LSI pin pull-up control register 0	PUPR0	R/W	H'5D60 FFFF	H'E606 0100	32	—
LSI pin pull-up control register 1	PUPR1	R/W	H'7FD8 3FF3	H'E606 0104	32	—
LSI pin pull-up control register 2	PUPR2	R/W	H'27FF FFFF	H'E606 0108	32	—
LSI pin pull-up control register 3	PUPR3	R/W	H'FFFF FFFF	H'E606 010C	32	—
LSI pin pull-up control register 4	PUPR4	R/W	H'FFFF FFFF	H'E606 0110	32	—
LSI pin pull-up control register 5	PUPR5	R/W	H'00FF FF1F	H'E606 0114	32	—
LSI pin pull-up control register 6	PUPR6	R/W	H'0000 0000	H'E606 0118	32	—
SD control register 0	IOCTRL0	R/W	H'FFFF FFFF	H'E606 0060	32	—
SD control register 1	IOCTRL1	R/W	H'FFFF F000	H'E606 0064	32	—
TDSEL control register	IOCTRL2	R/W	H'0000 0000	H'E606 0068	32	—
POC control register	IOCTRL3	R/W	H'FFFF FFFF	H'E606 006C	32	—
IICDVFS and TDBG IO cell control register	IOCTRL7	R/W	H'0000 0000	H'E606 0070	32	—

5.3 Register Description

[Legend]

Initial value:	Register value after a reset
— :	Undefined value
R/W:	Readable/writable. The written value can be read.
R:	Read-only. The write value should always be 0.
R/WC0:	Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.
R/WC1:	Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.
W:	Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.
—/W:	Write-only. The read value is undefined.

All the bits are active high unless otherwise specified, and deactivated on reset.

All access to registers is made in longword units.

The write value to a reserved bit should always be 0.

5.3.1 LSI Multiplexed Pin Setting Mask Register (PMMR)

Function: PMMR enables/disables writing to the multiplexed pin setting registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PMMR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PMMR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: This register must be set before setting each of the GPIO/peripheral function select registers GPSR0 to GPSR6, peripheral function select registers IPSR0 to IPSR13, module select registers MOD_SEL, MOD_SEL2 and MOD_SEL3, IO cell control registers IOCTRL0 to IOCTRL3 and IOCTRL7.

5.3.2 GPIO/Peripheral Function Select Register 0 (GPSR0)

Function: GPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP0 [31]	GP0 [30]	GP0 [29]	GP0 [28]	GP0 [27]	GP0 [26]	GP0 [25]	GP0 [24]	GP0 [23]	GP0 [22]	GP0 [21]	GP0 [20]	GP0 [19]	GP0 [18]	GP0 [17]	GP0 [16]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP0 [15]	GP0 [14]	GP0 [13]	GP0 [12]	GP0 [11]	GP0 [10]	GP0 [9]	GP0 [8]	GP0 [7]	GP0 [6]	GP0 [5]	GP0 [4]	GP0 [3]	GP0 [2]	GP0 [1]	GP0 [0]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP0[31:0]	H'FFFF FFFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[0]	GP-0-0	peripheral function selected by IP0[23:22]
GP0[1]	GP-0-1	peripheral function selected by IP0[24]
GP0[2]	GP-0-2	peripheral function selected by IP0[25]
GP0[3]	GP-0-3	peripheral function selected by IP0[27:26]
GP0[4]	GP-0-4	peripheral function selected by IP0[29:28]
GP0[5]	GP-0-5	peripheral function selected by IP0[31:30]
GP0[6]	GP-0-6	peripheral function selected by IP1[1:0]
GP0[7]	GP-0-7	peripheral function selected by IP1[3:2]
GP0[8]	GP-0-8	peripheral function selected by IP1[5:4]
GP0[9]	GP-0-9	peripheral function selected by IP1[7:6]
GP0[10]	GP-0-10	peripheral function selected by IP1[10:8]
GP0[11]	GP-0-11	peripheral function selected by IP1[12:11]
GP0[12]	GP-0-12	peripheral function selected by IP1[14:13]
GP0[13]	GP-0-13	peripheral function selected by IP1[17:15]
GP0[14]	GP-0-14	peripheral function selected by IP1[19:18]
GP0[15]	GP-0-15	peripheral function selected by IP1[21:20]
GP0[16]	GP-0-16	peripheral function selected by IP1[23:22]
GP0[17]	GP-0-17	peripheral function selected by IP1[24]
GP0[18]	GP-0-18	A2
GP0[19]	GP-0-19	peripheral function selected by IP1[26]
GP0[20]	GP-0-20	peripheral function selected by IP1[27]
GP0[21]	GP-0-21	peripheral function selected by IP1[29:28]
GP0[22]	GP-0-22	peripheral function selected by IP1[31:30]
GP0[23]	GP-0-23	peripheral function selected by IP2[1:0]
GP0[24]	GP-0-24	peripheral function selected by IP2[3:2]
GP0[25]	GP-0-25	peripheral function selected by IP2[5:4]
GP0[26]	GP-0-26	peripheral function selected by IP2[7:6]
GP0[27]	GP-0-27	peripheral function selected by IP2[9:8]
GP0[28]	GP-0-28	peripheral function selected by IP2[11:10]
GP0[29]	GP-0-29	peripheral function selected by IP2[13:12]
GP0[30]	GP-0-30	peripheral function selected by IP2[15:14]
GP0[31]	GP-0-31	peripheral function selected by IP2[17:16]

5.3.3 GPIO/Peripheral Function Select Register 1 (GPSR1)

Function: GPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP1 [31]	GP1 [30]	GP1 [29]	GP1 [28]	GP1 [27]	GP1 [26]	GP1 [25]	GP1 [24]	GP1 [23]	GP1 [22]	GP1 [21]	GP1 [20]	GP1 [19]	GP1 [18]	GP1 [17]	GP1 [16]
Initial value:	0	0	0	0	0	0	0	0	1/0	1/0	1/0	0	1/0	1/0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP1 [15]	GP1 [14]	GP1 [13]	GP1 [12]	GP1 [11]	GP1 [10]	GP1 [9]	GP1 [8]	GP1 [7]	GP1 [6]	GP1 [5]	GP1 [4]	GP1 [3]	GP1 [2]	GP1 [1]	GP1 [0]
Initial value:	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP1[31:0]	H'00EC 0FFF (when md[3:1] = 000), H'0000 0000 (when md[3:1] ≠ 000)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[0]	GP-1-0	Peripheral function selected by IP2[20:18]
GP1[1]	GP-1-1	Peripheral function selected by IP2[23:21]
GP1[2]	GP-1-2	Peripheral function selected by IP2[26:24]
GP1[3]	GP-1-3	Peripheral function selected by IP2[29:27]
GP1[4]	GP-1-4	Peripheral function selected by IP2[31:30]
GP1[5]	GP-1-5	Peripheral function selected by IP3[1:0]
GP1[6]	GP-1-6	Peripheral function selected by IP3[3:2]
GP1[7]	GP-1-7	Peripheral function selected by IP3[5:4]
GP1[8]	GP-1-8	Peripheral function selected by IP3[7:6]
GP1[9]	GP-1-9	Peripheral function selected by IP3[9:8]
GP1[10]	GP-1-10	Peripheral function selected by IP3[10]
GP1[11]	GP-1-11	Peripheral function selected by IP3[11]
GP1[12]	GP-1-12	Peripheral function selected by IP3[12]
GP1[13]	GP-1-13	Peripheral function selected by IP3[14:13]
GP1[14]	GP-1-14	Peripheral function selected by IP3[17:15]
GP1[15]	GP-1-15	Peripheral function selected by IP3[20:18]
GP1[16]	GP-1-16	Peripheral function selected by IP3[23:21]
GP1[17]	GP-1-17	Peripheral function selected by IP3[26:24]
GP1[18]	GP-1-18	Peripheral function selected by IP3[29:27]
GP1[19]	GP-1-19	Peripheral function selected by IP3[30]
GP1[20]	GP-1-20	Peripheral function selected by IP3[31]
GP1[21]	GP-1-21	WE0_N

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[22]	GP-1-22	WE1_N
GP1[23]	GP-1-23	Peripheral function selected by IP4[1:0]
GP1[24]	GP-1-24	Peripheral function selected by IP7[31]
GP1[25]	GP-1-25	DACK0
GP1[26]	-	-
GP1[27]	-	-
GP1[28]	-	-
GP1[29]	-	-
GP1[30]	-	-
GP1[31]	-	-

5.3.4 GPIO/Peripheral Function Select Register 2 (GPSR2)

Function: GPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP2 [31]	GP2 [30]	GP2 [29]	GP2 [28]	GP2 [27]	GP2 [26]	GP2 [25]	GP2 [24]	GP2 [23]	GP2 [22]	GP2 [21]	GP2 [20]	GP2 [19]	GP2 [18]	GP2 [17]	GP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP2 [15]	GP2 [14]	GP2 [13]	GP2 [12]	GP2 [11]	GP2 [10]	GP2 [9]	GP2 [8]	GP2 [7]	GP2 [6]	GP2 [5]	GP2 [4]	GP2 [3]	GP2 [2]	GP2 [1]	GP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP2[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP2[0]	GP-2-0	Peripheral function selected by IP4[4:2]
GP2[1]	GP-2-1	Peripheral function selected by IP4[7:5]
GP2[2]	GP-2-2	Peripheral function selected by IP4[9:8]
GP2[3]	GP-2-3	Peripheral function selected by IP4[11:10]
GP2[4]	GP-2-4	Peripheral function selected by IP4[13:12]
GP2[5]	GP-2-5	Peripheral function selected by IP4[15:14]
GP2[6]	GP-2-6	Peripheral function selected by IP4[17:16]
GP2[7]	GP-2-7	Peripheral function selected by IP4[19:18]
GP2[8]	GP-2-8	Peripheral function selected by IP4[22:20]
GP2[9]	GP-2-9	Peripheral function selected by IP4[25:23]
GP2[10]	GP-2-10	Peripheral function selected by IP4[27:26]
GP2[11]	GP-2-11	Peripheral function selected by IP4[29:28]
GP2[12]	GP-2-12	Peripheral function selected by IP4[31:30]
GP2[13]	GP-2-13	Peripheral function selected by IP5[1:0]
GP2[14]	GP-2-14	Peripheral function selected by IP5[3:2]
GP2[15]	GP-2-15	Peripheral function selected by IP5[5:4]
GP2[16]	GP-2-16	Peripheral function selected by IP5[8:6]
GP2[17]	GP-2-17	Peripheral function selected by IP5[11:9]
GP2[18]	GP-2-18	Peripheral function selected by IP5[13:12]
GP2[19]	GP-2-19	Peripheral function selected by IP5[15:14]
GP2[20]	GP-2-20	Peripheral function selected by IP5[17:16]
GP2[21]	GP-2-21	Peripheral function selected by IP5[19:18]
GP2[22]	GP-2-22	Peripheral function selected by IP5[21:20]
GP2[23]	GP-2-23	Peripheral function selected by IP5[23:22]
GP2[24]	GP-2-24	Peripheral function selected by IP5[25:24]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP2[25]	GP-2-25	Peripheral function selected by IP5[27:26]
GP2[26]	GP-2-26	Peripheral function selected by IP5[29:28]
GP2[27]	GP-2-27	Peripheral function selected by IP5[31:30]
GP2[28]	GP-2-28	Peripheral function selected by IP6[1:0]
GP2[29]	GP-2-29	Peripheral function selected by IP6[3:2]
GP2[30]	GP-2-30	Peripheral function selected by IP6[5:4]
GP2[31]	GP-2-31	Peripheral function selected by IP6[7:6]

5.3.5 GPIO/Peripheral Function Select Register 3 (GPSR3)

Function: GPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP3 [31]	GP3 [30]	GP3 [29]	GP3 [28]	GP3 [27]	GP3 [26]	GP3 [25]	GP3 [24]	GP3 [23]	GP3 [22]	GP3 [21]	GP3 [20]	GP3 [19]	GP3 [18]	GP3 [17]	GP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP3 [15]	GP3 [14]	GP3 [13]	GP3 [12]	GP3 [11]	GP3 [10]	GP3 [9]	GP3 [8]	GP3 [7]	GP3 [6]	GP3 [5]	GP3 [4]	GP3 [3]	GP3 [2]	GP3 [1]	GP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP3[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[0]	GP-3-0	Peripheral function selected by IP6[8]
GP3[1]	GP-3-1	Peripheral function selected by IP6[9]
GP3[2]	GP-3-2	Peripheral function selected by IP6[10]
GP3[3]	GP-3-3	Peripheral function selected by IP6[11]
GP3[4]	GP-3-4	Peripheral function selected by IP6[12]
GP3[5]	GP-3-5	Peripheral function selected by IP6[13]
GP3[6]	GP-3-6	Peripheral function selected by IP6[14]
GP3[7]	GP-3-7	Peripheral function selected by IP6[15]
GP3[8]	GP-3-8	Peripheral function selected by IP6[16]
GP3[9]	GP-3-9	Peripheral function selected by IP6[19:17]
GP3[10]	GP-3-10	Peripheral function selected by IP6[22:20]
GP3[11]	GP-3-11	Peripheral function selected by IP6[25:23]
GP3[12]	GP-3-12	Peripheral function selected by IP6[28:26]
GP3[13]	GP-3-13	Peripheral function selected by IP6[31:29]
GP3[14]	GP-3-14	Peripheral function selected by IP7[2:0]
GP3[15]	GP-3-15	Peripheral function selected by IP7[5:3]
GP3[16]	GP-3-16	Peripheral function selected by IP7[8:6]
GP3[17]	GP-3-17	Peripheral function selected by IP7[11:9]
GP3[18]	GP-3-18	Peripheral function selected by IP7[14:12]
GP3[19]	GP-3-19	Peripheral function selected by IP7[17:15]
GP3[20]	GP-3-20	Peripheral function selected by IP7[20:18]
GP3[21]	GP-3-21	Peripheral function selected by IP7[23:21]
GP3[22]	GP-3-22	Peripheral function selected by IP7[26:24]
GP3[23]	GP-3-23	Peripheral function selected by IP7[29:27]
GP3[24]	GP-3-24	Peripheral function selected by IP8[2:0]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP3[25]	GP-3-25	Peripheral function selected by IP8[5:3]
GP3[26]	GP-3-26	Peripheral function selected by IP8[8:6]
GP3[27]	GP-3-27	Peripheral function selected by IP8[11:9]
GP3[28]	GP-3-28	Peripheral function selected by IP8[14:12]
GP3[29]	GP-3-29	Peripheral function selected by IP8[16:15]
GP3[30]	GP-3-30	Peripheral function selected by IP8[19:17]
GP3[31]	GP-3-31	Peripheral function selected by IP8[22:20]

5.3.6 GPIO/Peripheral Function Select Register 4 (GPSR4)

Function: GPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP4 [31]	GP4 [30]	GP4 [29]	GP4 [28]	GP4 [27]	GP4 [26]	GP4 [25]	GP4 [24]	GP4 [23]	GP4 [22]	GP4 [21]	GP4 [20]	GP4 [19]	GP4 [18]	GP4 [17]	GP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP4 [15]	GP4 [14]	GP4 [13]	GP4 [12]	GP4 [11]	GP4 [10]	GP4 [9]	GP4 [8]	GP4 [7]	GP4 [6]	GP4 [5]	GP4 [4]	GP4 [3]	GP4 [2]	GP4 [1]	GP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP4[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP4[0]	GP-4-0	Peripheral function selected by IP8[25:23]
GP4[1]	GP-4-1	Peripheral function selected by IP8[28:26]
GP4[2]	GP-4-2	Peripheral function selected by IP8[31:29]
GP4[3]	GP-4-3	Peripheral function selected by IP9[2:0]
GP4[4]	GP-4-4	Peripheral function selected by IP9[5:3]
GP4[5]	GP-4-5	Peripheral function selected by IP9[8:6]
GP4[6]	GP-4-6	Peripheral function selected by IP9[11:9]
GP4[7]	GP-4-7	Peripheral function selected by IP9[14:12]
GP4[8]	GP-4-8	Peripheral function selected by IP9[16:15]
GP4[9]	GP-4-9	Peripheral function selected by IP9[18:17]
GP4[10]	GP-4-10	Peripheral function selected by IP9[21:19]
GP4[11]	GP-4-11	Peripheral function selected by IP9[24:22]
GP4[12]	GP-4-12	Peripheral function selected by IP9[27:25]
GP4[13]	GP-4-13	Peripheral function selected by IP9[30:28]
GP4[14]	GP-4-14	Peripheral function selected by IP10[2:0]
GP4[15]	GP-4-15	Peripheral function selected by IP10[5:3]
GP4[16]	GP-4-16	Peripheral function selected by IP10[8:6]
GP4[17]	GP-4-17	Peripheral function selected by IP10[11:9]
GP4[18]	GP-4-18	Peripheral function selected by IP10[14:12]
GP4[19]	GP-4-19	Peripheral function selected by IP10[17:15]
GP4[20]	GP-4-20	Peripheral function selected by IP10[20:18]
GP4[21]	GP-4-21	Peripheral function selected by IP10[23:21]
GP4[22]	GP-4-22	Peripheral function selected by IP10[26:24]
GP4[23]	GP-4-23	Peripheral function selected by IP10[29:27]
GP4[24]	GP-4-24	Peripheral function selected by IP10[31:30]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP4[25]	GP-4-25	Peripheral function selected by IP11[2:0]
GP4[26]	GP-4-26	Peripheral function selected by IP11[5:3]
GP4[27]	GP-4-27	Peripheral function selected by IP11[7:6]
GP4[28]	GP-4-28	Peripheral function selected by IP11[10:8]
GP4[29]	GP-4-29	Peripheral function selected by IP11[13:11]
GP4[30]	GP-4-30	Peripheral function selected by IP11[15:14]
GP4[31]	GP-4-31	Peripheral function selected by IP11[17:16]

5.3.7 GPIO/Peripheral Function Select Register 5 (GPSR5)

Function: GPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP5 [31]	GP5 [30]	GP5 [29]	GP5 [28]	GP5 [27]	GP5 [26]	GP5 [25]	GP5 [24]	GP5 [23]	GP5 [22]	GP5 [21]	GP5 [20]	GP5 [19]	GP5 [18]	GP5 [17]	GP5 [16]
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP5 [15]	GP5 [14]	GP5 [13]	GP5 [12]	GP5 [11]	GP5 [10]	GP5 [9]	GP5 [8]	GP5 [7]	GP5 [6]	GP5 [5]	GP5 [4]	GP5 [3]	GP5 [2]	GP5 [1]	GP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP5[31:0]	H'0F00 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[0]	GP-5-0	Peripheral function selected by IP11[20:18]
GP5[1]	GP-5-1	Peripheral function selected by IP11[23:21]
GP5[2]	GP-5-2	Peripheral function selected by IP11[26:24]
GP5[3]	GP-5-3	Peripheral function selected by IP11[29:27]
GP5[4]	GP-5-4	Peripheral function selected by IP12[2:0]
GP5[5]	GP-5-5	Peripheral function selected by IP12[5:3]
GP5[6]	GP-5-6	Peripheral function selected by IP12[8:6]
GP5[7]	GP-5-7	Peripheral function selected by IP12[10:9]
GP5[8]	GP-5-8	Peripheral function selected by IP12[12:11]
GP5[9]	GP-5-9	Peripheral function selected by IP12[14:13]
GP5[10]	GP-5-10	Peripheral function selected by IP12[17:15]
GP5[11]	GP-5-11	Peripheral function selected by IP12[20:18]
GP5[12]	GP-5-12	Peripheral function selected by IP12[23:21]
GP5[13]	GP-5-13	Peripheral function selected by IP12[26:24]
GP5[14]	GP-5-14	Peripheral function selected by IP12[29:27]
GP5[15]	GP-5-15	Peripheral function selected by IP13[2:0]
GP5[16]	GP-5-16	Peripheral function selected by IP13[5:3]
GP5[17]	GP-5-17	Peripheral function selected by IP13[8:6]
GP5[18]	GP-5-18	Peripheral function selected by IP13[11:9]
GP5[19]	GP-5-19	Peripheral function selected by IP13[14:12]
GP5[20]	GP-5-20	Peripheral function selected by IP13[17:15]
GP5[21]	GP-5-21	Peripheral function selected by IP13[20:18]
GP5[22]	GP-5-22	Peripheral function selected by IP13[23:21]
GP5[23]	GP-5-23	Peripheral function selected by IP13[26:24]
GP5[24]	GP-5-24	USB0_PWEN

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP5[25]	GP-5-25	USB0_OVC
GP5[26]	GP-5-26	USB1_PWEN
GP5[27]	GP-5-27	USB1_OVC
GP5[28]	-	-
GP5[29]	-	-
GP5[30]	-	-
GP5[31]	-	-

5.3.8 GPIO/Peripheral Function Select Register 6 (GPSR6)

Function: GPSR6 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP6 [31]	GP6 [30]	GP6 [29]	GP6 [28]	GP6 [27]	GP6 [26]	GP6 [25]	GP6 [24]	GP6 [23]	GP6 [22]	GP6 [21]	GP6 [20]	GP6 [19]	GP6 [18]	GP6 [17]	GP6 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP6 [15]	GP6 [14]	GP6 [13]	GP6 [12]	GP6 [11]	GP6 [10]	GP6 [9]	GP6 [8]	GP6 [7]	GP6 [6]	GP6 [5]	GP6 [4]	GP6 [3]	GP6 [2]	GP6 [1]	GP6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP6[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP6[0]	GP-6-0	SD0_CLK
GP6[1]	GP-6-1	SD0_CMD
GP6[2]	GP-6-2	SD0_DATA0
GP6[3]	GP-6-3	SD0_DATA1
GP6[4]	GP-6-4	SD0_DATA2
GP6[5]	GP-6-5	SD0_DATA3
GP6[6]	GP-6-6	SD0_CD
GP6[7]	GP-6-7	SD0_WP
GP6[8]	GP-6-8	SD1_CLK
GP6[9]	GP-6-9	SD1_CMD
GP6[10]	GP-6-10	SD1_DATA0
GP6[11]	GP-6-11	SD1_DATA1
GP6[12]	GP-6-12	SD1_DATA2
GP6[13]	GP-6-13	SD1_DATA3
GP6[14]	GP-6-14	Peripheral function selected by IP0[0]
GP6[15]	GP-6-15	Peripheral function selected by IP0[9:8]
GP6[16]	GP-6-16	Peripheral function selected by IP0[10]
GP6[17]	GP-6-17	Peripheral function selected by IP0[11]
GP6[18]	GP-6-18	Peripheral function selected by IP0[12]
GP6[19]	GP-6-19	Peripheral function selected by IP0[13]
GP6[20]	GP-6-20	Peripheral function selected by IP0[14]
GP6[21]	GP-6-21	Peripheral function selected by IP0[15]
GP6[22]	GP-6-22	Peripheral function selected by IP0[16]
GP6[23]	GP-6-23	Peripheral function selected by IP0[17]
GP6[24]	GP-6-24	Peripheral function selected by IP0[19:18]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP6[25]	GP-6-25	Peripheral function selected by IP0[21:20]
GP6[26]	-	-
GP6[27]	-	-
GP6[28]	-	-
GP6[29]	-	-
GP6[30]	-	-
GP6[31]	-	-

5.3.9 Peripheral Function Select Register 0 (IPSR0)

Function: IPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP0 [31]	IP0 [30]	IP0 [29]	IP0 [28]	IP0 [27]	IP0 [26]	IP0 [25]	IP0 [24]	IP0 [23]	IP0 [22]	IP0 [21]	IP0 [20]	IP0 [19]	IP0 [18]	IP0 [17]	IP0 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP0 [15]	IP0 [14]	IP0 [13]	IP0 [12]	IP0 [11]	IP0 [10]	IP0 [9]	IP0 [8]	IP0 [7]	IP0 [6]	IP0 [5]	IP0 [4]	IP0 [3]	IP0 [2]	IP0 [1]	IP0 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP0[0]	SD1_CD	CAN0_RX	-	-	-	-	-
IP0[9:8]	SD1_WP	IRQ7	CAN0_TX	-	-	-	-
IP0[10]	MMC_CLK	SD2_CLK	-	-	-	-	-
IP0[11]	MMC_CMD	SD2_CMD	-	-	-	-	-
IP0[12]	MMC_D0	SD2_DATA0	-	-	-	-	-
IP0[13]	MMC_D1	SD2_DATA1	-	-	-	-	-
IP0[14]	MMC_D2	SD2_DATA2	-	-	-	-	-
IP0[15]	MMC_D3	SD2_DATA3	-	-	-	-	-
IP0[16]	MMC_D4	SD2_CD	-	-	-	-	-
IP0[17]	MMC_D5	SD2_WP	-	-	-	-	-
IP0[19:18]	MMC_D6	SCIF0_RXD	I2C2_SCL_B	CAN1_RX	-	-	-
IP0[21:20]	MMC_D7	SCIF0_TXD	I2C2_SDA_B	CAN1_TX	-	-	-
IP0[23:22]	D0	SCIFA3_SCK_B	IRQ4	-	-	-	-
IP0[24]	D1	SCIFA3_RXD_B	-	-	-	-	-
IP0[25]	D2	SCIFA3_TXD_B	-	-	-	-	-
IP0[27:26]	D3	I2C3_SCL_B	SCIF5_RXD_B	-	-	-	-
IP0[29:28]	D4	I2C3_SDA_B	SCIF5_TXD_B	-	-	-	-
IP0[31:30]	D5	SCIF4_RXD_B	I2C0_SCL_D	-	-	-	-

Legend: - Setting prohibited

5.3.10 Peripheral Function Select Register 1 (IPSR1)

Function: IPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP1 [31]	IP1 [30]	IP1 [29]	IP1 [28]	IP1 [27]	IP1 [26]	IP1 [25]	IP1 [24]	IP1 [23]	IP1 [22]	IP1 [21]	IP1 [20]	IP1 [19]	IP1 [18]	IP1 [17]	IP1 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP1 [15]	IP1 [14]	IP1 [13]	IP1 [12]	IP1 [11]	IP1 [10]	IP1 [9]	IP1 [8]	IP1 [7]	IP1 [6]	IP1 [5]	IP1 [4]	IP1 [3]	IP1 [2]	IP1 [1]	IP1 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP1[1:0]	D6	SCIF4_TXD_B	I2C0_SDA_D	-	-	-	-	-
IP1[3:2]	D7	IRQ3	TCLK1	PWM6_B	-	-	-	-
IP1[5:4]	D8	HSCIF2_HRX	I2C1_SCL_B	-	-	-	-	-
IP1[7:6]	D9	HSCIF2_HTX	I2C1_SDA_B	-	-	-	-	-
IP1[10:8]	D10	HSCIF2_HSCK	SCIF1_SCK_C	IRQ6	PWM5_C	-	-	-
IP1[12:11]	D11	HSCIF2_HCTS_N	SCIF1_RXD_C	I2C1_SCL_D	-	-	-	-
IP1[14:13]	D12	HSCIF2_HRTS_N	SCIF1_TXD_C	I2C1_SDA_D	-	-	-	-
IP1[17:15]	D13	SCIFA1_SCK	Reserved	PWM2_C	TCLK2_B	-	-	-
IP1[19:18]	D14	SCIFA1_RXD	I2C5_SCL_B	-	-	-	-	-
IP1[21:20]	D15	SCIFA1_TXD	I2C5_SDA_B	-	-	-	-	-
IP1[23:22]	A0	SCIFB1_SCK	PWM3_B	-	-	-	-	-
IP1[24]	A1	SCIFB1_TXD	-	-	-	-	-	-
IP1[26]	A3	SCIFB0_SCK	-	-	-	-	-	-
IP1[27]	A4	SCIFB0_TXD	-	-	-	-		
IP1[29:28]	A5	SCIFB0_RXD	PWM4_B	TPUTO3_C	-	-	-	-
IP1[31:30]	A6	SCIFB0_CTS_N	SCIFA4_RXD_B	TPUTO2_C	-	-	-	-

Legend: - Setting prohibited

5.3.11 Peripheral Function Select Register 2 (IPSR2)

Function: IPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP2 [31]	IP2 [30]	IP2 [29]	IP2 [28]	IP2 [27]	IP2 [26]	IP2 [25]	IP2 [24]	IP2 [23]	IP2 [22]	IP2 [21]	IP2 [20]	IP2 [19]	IP2 [18]	IP2 [17]	IP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP2 [15]	IP2 [14]	IP2 [13]	IP2 [12]	IP2 [11]	IP2 [10]	IP2 [9]	IP2 [8]	IP2 [7]	IP2 [6]	IP2 [5]	IP2 [4]	IP2 [3]	IP2 [2]	IP2 [1]	IP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP2[1:0]	A7	SCIFB0_RTS_N	SCIFA4_TXD_B	-	-	-	-	-	-
IP2[3:2]	A8	MSIOF1_RXD	SCIFA0_RXD_B	-	-	-	-	-	-
IP2[5:4]	A9	MSIOF1_TXD	SCIFA0_TXD_B	-	-	-	-	-	-
IP2[7:6]	A10	MSIOF1_SCK	IIC0_SCL_B (I2C6)	-	-	-	-	-	-
IP2[9:8]	A11	MSIOF1_SYNC	IIC0_SDA_B (I2C6)	-	-	-	-	-	-
IP2[11:10]	A12	MSIOF1_SS1	SCIFA5_RXD_B	-	-	-	-	-	-
IP2[13:12]	A13	MSIOF1_SS2	SCIFA5_TXD_B	-	-	-	-	-	-
IP2[15:14]	A14	MSIOF2_RXD	HSCIF0_HRX_B	DREQ1_N	-	-	-	-	-
IP2[17:16]	A15	MSIOF2_TXD	HSCIF0_HTX_B	DACK1	-	-	-	-	-
IP2[20:18]	A16	MSIOF2_SCK	HSCIF0_HSCK_B	Reserved	Reserved	CAN_CLK_C	TPUTO2_B	-	-
IP2[23:21]	A17	MSIOF2_SYNC	SCIF4_RXD_E	CAN1_RX_B	Reserved	-	-	-	-
IP2[26:24]	A18	MSIOF2_SS1	SCIF4_TXD_E	CAN1_TX_B	Reserved	-	-	-	-
IP2[29:27]	A19	MSIOF2_SS2	PWM4	TPUTO2	Reserved	-	-	-	-
IP2[31:30]	A20	SPCLK	Reserved	-	-	-	-	-	-

Legend: - Setting prohibited

5.3.12 Peripheral Function Select Register 3 (IPSR3)

Function: IPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP3 [31]	IP3 [30]	IP3 [29]	IP3 [28]	IP3 [27]	IP3 [26]	IP3 [25]	IP3 [24]	IP3 [23]	IP3 [22]	IP3 [21]	IP3 [20]	IP3 [19]	IP3 [18]	IP3 [17]	IP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP3 [15]	IP3 [14]	IP3 [13]	IP3 [12]	IP3 [11]	IP3 [10]	IP3 [9]	IP3 [8]	IP3 [7]	IP3 [6]	IP3 [5]	IP3 [4]	IP3 [3]	IP3 [2]	IP3 [1]	IP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)	Others (Set Value = H'8 to H'F)
IP3[1:0]	A21	MOSI_IO0	Reserved	-	-	-	-	-	-
IP3[3:2]	A22	MISO_IO1	Reserved	ATADIR1_N	-	-	-	-	-
IP3[5:4]	A23	IO2	Reserved	ATAWR1_N	-	-	-	-	-
IP3[7:6]	A24	IO3	EX_WAIT2	-	-	-	-	-	-
IP3[9:8]	A25	SSL	ATARD1_N	-	-	-	-	-	-
IP3[10]	CS0_N	VI1_DATA8	-	-	-	-	-	-	-
IP3[11]	CS1_N_A26	VI1_DATA9	-	-	-	-	-	-	-
IP3[12]	EX_CS0_N	VI1_DATA10	-	-	-	-	-	-	-
IP3[14:13]	EX_CS1_N	TPUTO3_B	SCIFB2_RXD	VI1_DATA11	-	-	-	-	-
IP3[17:15]	EX_CS2_N	PWM0	SCIF4_RXD_C	Reserved	Reserved	TPUTO3	SCIFB2_TXD	Reserved	-
IP3[20:18]	EX_CS3_N	SCIFA2_SCK	SCIF4_TXD_C	Reserved	Reserved	Reserved	SCIFB2_SCK	Reserved	-
IP3[23:21]	EX_CS4_N	SCIFA2_RXD	I2C2_SCL_E	Reserved	Reserved	Reserved	SCIFB2_CTS_N	Reserved	-
IP3[26:24]	EX_CS5_N	SCIFA2_TXD	I2C2_SDA_E	Reserved	Reserved	Reserved	SCIFB2_RTS_N	Reserved	-
IP3[29:27]	BS_N	DRACK0	PWM1_C	TPUTO0_C	ATACS01_N	Reserved	-	-	-
IP3[30]	RD_N	ATACS11_N	-	-	-	-	-	-	-
IP3[31]	RD_WR_N	ATAG1_N	-	-	-	-	-	-	-

Legend: - Setting prohibited

5.3.13 Peripheral Function Select Register 4 (IPSR4)

Function: IPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP4 [31]	IP4 [30]	IP4 [29]	IP4 [28]	IP4 [27]	IP4 [26]	IP4 [25]	IP4 [24]	IP4 [23]	IP4 [22]	IP4 [21]	IP4 [20]	IP4 [19]	IP4 [18]	IP4 [17]	IP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP4 [15]	IP4 [14]	IP4 [13]	IP4 [12]	IP4 [11]	IP4 [10]	IP4 [9]	IP4 [8]	IP4 [7]	IP4 [6]	IP4 [5]	IP4 [4]	IP4 [3]	IP4 [2]	IP4 [1]	IP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP4[1:0]	EX_WAIT0	CAN_CLK_B	SCIF_CLK	Reserved	-	-	-
IP4[4:2]	DU0_DR0	Reserved	SCIF5_RXD_C	I2C2_SCL_D	Reserved	-	-
IP4[7:5]	DU0_DR1	Reserved	SCIF5_TXD_C	I2C2_SDA_D	Reserved	-	-
IP4[9:8]	DU0_DR2	Reserved	Reserved	-	-	-	-
IP4[11:10]	DU0_DR3	Reserved	Reserved	-	-	-	-
IP4[13:12]	DU0_DR4	Reserved	Reserved	-	-	-	-
IP4[15:14]	DU0_DR5	Reserved	Reserved	-	-	-	-
IP4[17:16]	DU0_DR6	Reserved	Reserved	-	-	-	-
IP4[19:18]	DU0_DR7	Reserved	Reserved	-	-	-	-
IP4[22:20]	DU0_DG0	Reserved	SCIFA0_RXD_C	I2C3_SCL_D	Reserved	-	-
IP4[25:23]	DU0_DG1	Reserved	SCIFA0_TXD_C	I2C3_SDA_D	Reserved	-	-
IP4[27:26]	DU0_DG2	Reserved	Reserved	-	-	-	-
IP4[29:28]	DU0_DG3	Reserved	Reserved	-	-	-	-
IP4[31:30]	DU0_DG4	Reserved	Reserved	-	-	-	-

Legend: - Setting prohibited

5.3.14 Peripheral Function Select Register 5 (IPSR5)

Function: IPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP5 [31]	IP5 [30]	IP5 [29]	IP5 [28]	IP5 [27]	IP5 [26]	IP5 [25]	IP5 [24]	IP5 [23]	IP5 [22]	IP5 [21]	IP5 [20]	IP5 [19]	IP5 [18]	IP5 [17]	IP5 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP5 [15]	IP5 [14]	IP5 [13]	IP5 [12]	IP5 [11]	IP5 [10]	IP5 [9]	IP5 [8]	IP5 [7]	IP5 [6]	IP5 [5]	IP5 [4]	IP5 [3]	IP5 [2]	IP5 [1]	IP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Others (Set Value = H'6 to H'F)
IP5[1:0]	DU0_DG5	Reserved	Reserved	-	-	-	-
IP5[3:2]	DU0_DG6	Reserved	Reserved	-	-	-	-
IP5[5:4]	DU0_DG7	Reserved	Reserved	-	-	-	-
IP5[8:6]	DU0_DB0	Reserved	SCIFA4_RXD_C	I2C4_SCL_D	CAN0_RX_C	Reserved	-
IP5[11:9]	DU0_DB1	Reserved	SCIFA4_TXD_C	I2C4_SDA_D	CAN0_TX_C	Reserved	-
IP5[13:12]	DU0_DB2	Reserved	Reserved	-	-	-	-
IP5[15:14]	DU0_DB3	Reserved	Reserved	-	-	-	-
IP5[17:16]	DU0_DB4	Reserved	Reserved	-	-	-	-
IP5[19:18]	DU0_DB5	Reserved	Reserved	-	-	-	-
IP5[21:20]	DU0_DB6	Reserved	Reserved	-	-	-	-
IP5[23:22]	DU0_DB7	Reserved	Reserved	-	-	-	-
IP5[25:24]	DU0_DOTCLKIN	Reserved	Reserved	-	-	-	-
IP5[27:26]	DU0_DOTCLKOUT0	Reserved	Reserved	-	-	-	-
IP5[29:28]	DU0_DOTCLKOUT1	Reserved	Reserved	-	-	-	-
IP5[31:30]	DU0_EXHSYNC_DU0_HSYNC	Reserved	Reserved	-	-	-	-

Legend: - Setting prohibited

5.3.15 Peripheral Function Select Register 6 (IPSR6)

Function: IPSR6 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP6 [31]	IP6 [30]	IP6 [29]	IP6 [28]	IP6 [27]	IP6 [26]	IP6 [25]	IP6 [24]	IP6 [23]	IP6 [22]	IP6 [21]	IP6 [20]	IP6 [19]	IP6 [18]	IP6 [17]	IP6 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP6 [15]	IP6 [14]	IP6 [13]	IP6 [12]	IP6 [11]	IP6 [10]	IP6 [9]	IP6 [8]	IP6 [7]	IP6 [6]	IP6 [5]	IP6 [4]	IP6 [3]	IP6 [2]	IP6 [1]	IP6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Notes: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Others (Set Value = H'7 to H'F)
IP6[1:0]	DU0_EXVSYNC_DU0_VSYNC	Reserved	Reserved	-	-	-	-	-
IP6[3:2]	DU0_EXODDF_DU0_ODDF_DISP_CDE	Reserved	Reserved	-	-	-	-	-
IP6[5:4]	DU0_DISP	Reserved	Reserved	-	-	-	-	-
IP6[7:6]	DU0_CDE	Reserved	Reserved	-	-	-	-	-
IP6[8]	VI0_CLK	AVB_RX_CLK	-	-	-	-	-	-
IP6[9]	VI0_DATA0_VI0_B0	AVB_RX_DV	-	-	-	-	-	-
IP6[10]	VI0_DATA1_VI0_B1	AVB_RXD0	-	-	-	-	-	-
IP6[11]	VI0_DATA2_VI0_B2	AVB_RXD1	-	-	-	-	-	-
IP6[12]	VI0_DATA3_VI0_B3	AVB_RXD2	-	-	-	-	-	-
IP6[13]	VI0_DATA4_VI0_B4	AVB_RXD3	-	-	-	-	-	-
IP6[14]	VI0_DATA5_VI0_B5	AVB_RXD4	-	-	-	-	-	-
IP6[15]	VI0_DATA6_VI0_B6	AVB_RXD5	-	-	-	-	-	-
IP6[16]	VI0_DATA7_VI0_B7	AVB_RXD6	-	-	-	-	-	-
IP6[19:17]	VI0_CLKENB	I2C3_SCL	SCIFA5_RXD_C	Reserved	AVB_RXD7	-	-	-
IP6[22:20]	VI0_FIELD	I2C3_SDA	SCIFA5_TXD_C	Reserved	AVB_RX_ER	-	-	-
IP6[25:23]	VI0_HSYNC_N	SCIF0_RXD_B	I2C0_SCL_C	Reserved	AVB_COL	-	-	-
IP6[28:26]	VI0_VSYNC_N	SCIF0_TXD_B	I2C0_SDA_C	AUDIO_CLKOUT_B	AVB_TX_EN	-	-	-
IP6[31:29]	ETH_MDIO	VI0_G0	MSIOF2_RXD_B	I2C5_SCL_D	AVB_TX_CLK	Reserved	Reserved	-

Legend: - Setting prohibited

5.3.16 Peripheral Function Select Register 7 (IPSR7)

Function: IPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP7 [31]	IP7 [30]	IP7 [29]	IP7 [28]	IP7 [27]	IP7 [26]	IP7 [25]	IP7 [24]	IP7 [23]	IP7 [22]	IP7 [21]	IP7 [20]	IP7 [19]	IP7 [18]	IP7 [17]	IP7 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP7 [15]	IP7 [14]	IP7 [13]	IP7 [12]	IP7 [11]	IP7 [10]	IP7 [9]	IP7 [8]	IP7 [7]	IP7 [6]	IP7 [5]	IP7 [4]	IP7 [3]	IP7 [2]	IP7 [1]	IP7 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP7[2:0]	ETH_CRS_DV	VI0_G1	MSIOF2_TXD_B	I2C5_SDA_D	AVB_TXD0	Reserved	Reserved
IP7[5:3]	ETH_RX_ER	VI0_G2	MSIOF2_SCK_B	CAN0_RX_B	AVB_TXD1	Reserved	Reserved
IP7[8:6]	ETH_RXD0	VI0_G3	MSIOF2_SYNC_B	CAN0_TX_B	AVB_TXD2	Reserved	Reserved
IP7[11:9]	ETH_RXD1	VI0_G4	MSIOF2_SS1_B	SCIF4_RXD_D	AVB_TXD3	Reserved	-
IP7[14:12]	ETH_LINK	VI0_G5	MSIOF2_SS2_B	SCIF4_TXD_D	AVB_TXD4	Reserved	-
IP7[17:15]	ETH_REFCLK	VI0_G6	SCIF2_SCK_C	AVB_TXD5	SSI_SCK5_B	-	-
IP7[20:18]	ETH_TXD1	VI0_G7	SCIF2_RXD_C	IIC0_SCL_D	AVB_TXD6	SSI_WS5_B	-
IP7[23:21]	ETH_TX_EN	VI0_R0	SCIF2_TXD_C	IIC0_SDA_D	AVB_TXD7	SSI_SDATA5_B	-
IP7[26:24]	ETH_MAGIC	VI0_R1	SCIF3_SCK_B	AVB_TX_ER	SSI_SCK6_B	-	-
IP7[29:27]	ETH_TXD0	VI0_R2	SCIF3_RXD_B	I2C4_SCL_E	AVB_GTX_CLK	SSI_WS6_B	-
IP7[31]	DREQ0_N	SCIFB1_RXD	-	-	-	-	-

Legend: - Setting prohibited

5.3.17 Peripheral Function Select Register 8 (IPSR8)

Function: IPSR8 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP8 [31]	IP8 [30]	IP8 [29]	IP8 [28]	IP8 [27]	IP8 [26]	IP8 [25]	IP8 [24]	IP8 [23]	IP8 [22]	IP8 [21]	IP8 [20]	IP8 [19]	IP8 [18]	IP8 [17]	IP8 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP8 [15]	IP8 [14]	IP8 [13]	IP8 [12]	IP8 [11]	IP8 [10]	IP8 [9]	IP8 [8]	IP8 [7]	IP8 [6]	IP8 [5]	IP8 [4]	IP8 [3]	IP8 [2]	IP8 [1]	IP8 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)
IP8[2:0]	ETH_MDC	VI0_R3	SCIF3_TXD_B	I2C4_SDA_E	AVB_MDC	SSI_SDATA6_B	-	-
IP8[5:3]	HSCIF0_HRX	VI0_R4	I2C1_SCL_C	AUDIO_CLKA_B	AVB_MDIO	SSI_SCK78_B	-	-
IP8[8:6]	HSCIF0_HTX	VI0_R5	I2C1_SDA_C	AUDIO_CLKB_B	AVB_LINK	SSI_WS78_B	-	-
IP8[11:9]	HSCIF0_HCTS_N	VI0_R6	SCIF0_RXD_D	I2C0_SCL_E	AVB_MAGIC	SSI_SDATA7_B	-	-
IP8[14:12]	HSCIF0_HRTS_N	VI0_R7	SCIF0_TXD_D	I2C0_SDA_E	AVB_PHY_INT	SSI_SDATA8_B	-	-
IP8[16:15]	HSCIF0_HSCK	SCIF_CLK_B	AVB_CRS	AUDIO_CLKC_B	-	-	-	-
IP8[19:17]	I2C0_SCL	SCIF0_RXD_C	PWM5	TCLK1_B	AVB_GTXREFCLK	CAN1_RX_D	TPUTO0_B	-
IP8[22:20]	I2C0_SDA	SCIF0_TXD_C	TPUTO0	CAN_CLK	DVC_MUTE	CAN1_TX_D	-	-
IP8[25:23]	I2C1_SCL	SCIF4_RXD	PWM5_B	DU1_DR0	Reserved	Reserved	TPUTO1_B	-
IP8[28:26]	I2C1_SDA	SCIF4_TXD	IRQ5	DU1_DR1	Reserved	Reserved	Reserved	-
IP8[31:29]	MSIOF0_RXD	SCIF5_RXD	I2C2_SCL_C	DU1_DR2	Reserved	Reserved	Reserved	Reserved

Legend: - Setting prohibited

5.3.18 Peripheral Function Select Register 9 (IPSR9)

Function: IPSR9 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP9 [31]	IP9 [30]	IP9 [29]	IP9 [28]	IP9 [27]	IP9 [26]	IP9 [25]	IP9 [24]	IP9 [23]	IP9 [22]	IP9 [21]	IP9 [20]	IP9 [19]	IP9 [18]	IP9 [17]	IP9 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP9 [15]	IP9 [14]	IP9 [13]	IP9 [12]	IP9 [11]	IP9 [10]	IP9 [9]	IP9 [8]	IP9 [7]	IP9 [6]	IP9 [5]	IP9 [4]	IP9 [3]	IP9 [2]	IP9 [1]	IP9 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)
IP9[2:0]	MSIOF0_TXD	SCIF5_TXD	I2C2_SDA_C	DU1_DR3	Reserved	Reserved	Reserved	Reserved
IP9[5:3]	MSIOF0_SCK	IRQ0	Reserved	DU1_DR4	Reserved	TPUTO1_C	-	-
IP9[8:6]	MSIOF0_SYNC	PWM1	Reserved	DU1_DR5	Reserved	Reserved	-	-
IP9[11:9]	MSIOF0_SS1	SCIFA0_RXD	Reserved	DU1_DR6	Reserved	Reserved	Reserved	-
IP9[14:12]	MSIOF0_SS2	SCIFA0_TXD	Reserved	DU1_DR7	Reserved	Reserved	Reserved	-
IP9[16:15]	HSCIF1_HRX	I2C4_SCL	PWM6	DU1_DG0	-	-	-	-
IP9[18:17]	HSCIF1_HTX	I2C4_SDA	TPUTO1	DU1_DG1	-	-	-	-
IP9[21:19]	HSCIF1_HSCK	PWM2	Reserved	DU1_DG2	Reserved	Reserved	Reserved	-
IP9[24:22]	HSCIF1_HCTS_N	SCIFA4_RXD	Reserved	DU1_DG3	SSI_SCK1_B	Reserved	Reserved	-
IP9[27:25]	HSCIF1_HRTS_N	SCIFA4_TXD	Reserved	DU1_DG4	SSI_WS1_B	Reserved	Reserved	-
IP9[30:28]	SCIF1_SCK	PWM3	TCLK2	DU1_DG5	SSI_SDATA1_B	Reserved	Reserved	-

Legend: - Setting prohibited

5.3.19 Peripheral Function Select Register 10 (IPSR10)

Function: IPSR10 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP10 [31]	IP10 [30]	IP10 [29]	IP10 [28]	IP10 [27]	IP10 [26]	IP10 [25]	IP10 [24]	IP10 [23]	IP10 [22]	IP10 [21]	IP10 [20]	IP10 [19]	IP10 [18]	IP10 [17]	IP10 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP10 [15]	IP10 [14]	IP10 [13]	IP10 [12]	IP10 [11]	IP10 [10]	IP10 [9]	IP10 [8]	IP10 [7]	IP10 [6]	IP10 [5]	IP10 [4]	IP10 [3]	IP10 [2]	IP10 [1]	IP10 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)
IP10[2:0]	SCIF1_RXD	I2C5_SCL	DU1_DG6	SSI_SCK2_B	Reserved	Reserved	-	-
IP10[5:3]	SCIF1_TXD	I2C5_SDA	DU1_DG7	SSI_WS2_B	Reserved	Reserved	-	-
IP10[8:6]	SCIF2_RXD	IIC0_SCL	DU1_DB0	SSI_SDATA2_B	Reserved	Reserved	Reserved	-
IP10[11:9]	SCIF2_TXD	IIC0_SDA	DU1_DB1	SSI_SCK9_B	Reserved	Reserved	Reserved	-
IP10[14:12]	SCIF2_SCK	IRQ1	DU1_DB2	SSI_WS9_B	Reserved	Reserved	Reserved	-
IP10[17:15]	SCIF3_SCK	IRQ2	Reserved	DU1_DB3	SSI_SDATA9_B	Reserved	Reserved	Reserved
IP10[20:18]	SCIF3_RXD	I2C1_SCL_E	Reserved	DU1_DB4	AUDIO_CLKA_C	SSI_SCK4_B	Reserved	Reserved
IP10[23:21]	SCIF3_TXD	I2C1_SDA_E	Reserved	DU1_DB5	AUDIO_CLKB_C	SSI_WS4_B	Reserved	Reserved
IP10[26:24]	I2C2_SCL	SCIFA5_RXD	DU1_DB6	AUDIO_CLKC_C	SSI_SDATA4_B	Reserved	-	-
IP10[29:27]	I2C2_SDA	SCIFA5_TXD	DU1_DB7	AUDIO_CLKOUT_C	Reserved	-	-	-
IP10[31:30]	SSI_SCK5	SCIFA3_SCK	DU1_DOTCLKIN	Reserved	-	-	-	-

Legend: - Setting prohibited

5.3.20 Peripheral Function Select Register 11 (IPSR11)

Function: IPSR11 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP11 [31]	IP11 [30]	IP11 [29]	IP11 [28]	IP11 [27]	IP11 [26]	IP11 [25]	IP11 [24]	IP11 [23]	IP11 [22]	IP11 [21]	IP11 [20]	IP11 [19]	IP11 [18]	IP11 [17]	IP11 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP11 [15]	IP11 [14]	IP11 [13]	IP11 [12]	IP11 [11]	IP11 [10]	IP11 [9]	IP11 [8]	IP11 [7]	IP11 [6]	IP11 [5]	IP11 [4]	IP11 [3]	IP11 [2]	IP11 [1]	IP11 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)
IP11[2:0]	SSI_WS5	SCIFA3_RXD	I2C3_SCL_C	DU1_DOTCLKOUT0	Reserved	-
IP11[5:3]	SSI_SDATA5	SCIFA3_TXD	I2C3_SDA_C	DU1_DOTCLKOUT1	Reserved	-
IP11[7:6]	SSI_SCK6	SCIFA1_SCK_B	DU1_EXHSYNC_DU1_HSYNC	Reserved	-	-
IP11[10:8]	SSI_WS6	SCIFA1_RXD_B	I2C4_SCL_C	DU1_EXVSYNC_DU1_VSYNC	Reserved	-
IP11[13:11]	SSI_SDATA6	SCIFA1_TXD_B	I2C4_SDA_C	DU1_EXODDF_DU1_ODDF_DISP_CDE	Reserved	-
IP11[15:14]	SSI_SCK78	SCIFA2_SCK_B	I2C5_SDA_C	DU1_DISP	-	-
IP11[17:16]	SSI_WS78	SCIFA2_RXD_B	I2C5_SCL_C	DU1_CDE	-	-
IP11[20:18]	SSI_SDATA7	SCIFA2_TXD_B	IRQ8	AUDIO_CLKA_D	CAN_CLK_D	Reserved
IP11[23:21]	SSI_SCK0129	MSIOF1_RXD_B	SCIF5_RXD_D	Reserved	Reserved	Reserved
IP11[26:24]	SSI_WS0129	MSIOF1_TXD_B	SCIF5_TXD_D	Reserved	Reserved	-
IP11[29:27]	SSI_SDATA0	MSIOF1_SCK_B	PWM0_B	Reserved	Reserved	-

Legend: - Setting prohibited

5.3.21 Peripheral Function Select Register 12 (IPSR12)

Function: IPSR12 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP12 [31]	IP12 [30]	IP12 [29]	IP12 [28]	IP12 [27]	IP12 [26]	IP12 [25]	IP12 [24]	IP12 [23]	IP12 [22]	IP12 [21]	IP12 [20]	IP12 [19]	IP12 [18]	IP12 [17]	IP12 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP12 [15]	IP12 [14]	IP12 [13]	IP12 [12]	IP12 [11]	IP12 [10]	IP12 [9]	IP12 [8]	IP12 [7]	IP12 [6]	IP12 [5]	IP12 [4]	IP12 [3]	IP12 [2]	IP12 [1]	IP12 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP12[2:0]	SSI_SCK34	MSIOF1_SYNC_B	SCIFA1_SCK_C	Reserved	Reserved	DREQ1_N_B	-
IP12[5:3]	SSI_WS34	MSIOF1_SS1_B	SCIFA1_RXD_C	Reserved	CAN1_RX_C	DACK1_B	-
IP12[8:6]	SSI_SDATA3	MSIOF1_SS2_B	SCIFA1_TXD_C	Reserved	CAN1_TX_C	DREQ2_N	-
IP12[10:9]	SSI_SCK4	Reserved	Reserved	Reserved	-	-	-
IP12[12:11]	SSI_WS4	Reserved	Reserved	Reserved	-	-	-
IP12[14:13]	SSI_SDATA4	Reserved	Reserved	Reserved	-	-	-
IP12[17:15]	SSI_SDATA8	SCIF1_SCK_B	PWM1_B	IRQ9	Reserved	DACK2	ETH_MDIO_B
IP12[20:18]	SSI_SCK1	SCIF1_RXD_B	IIC0_SCL_C	VI1_CLK	CAN0_RX_D	Reserved	ETH_CRS_DV_B
IP12[23:21]	SSI_WS1	SCIF1_TXD_B	IIC0_SDA_C	VI1_DATA0	CAN0_TX_D	Reserved	ETH_RX_ER_B
IP12[26:24]	SSI_SDATA1	HSCIF1_HRX_B	VI1_DATA1	Reserved	ATAWR0_N	ETH_RXD0_B	-
IP12[29:27]	SSI_SCK2	HSCIF1_HTX_B	VI1_DATA2	Reserved	ATAG0_N	ETH_RXD1_B	-

Legend: - Setting prohibited

5.3.22 Peripheral Function Select Register 13 (IPSR13)

Function: IPSR13 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP13 [31]	IP13 [30]	IP13 [29]	IP13 [28]	IP13 [27]	IP13 [26]	IP13 [25]	IP13 [24]	IP13 [23]	IP13 [22]	IP13 [21]	IP13 [20]	IP13 [19]	IP13 [18]	IP13 [17]	IP13 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP13 [15]	IP13 [14]	IP13 [13]	IP13 [12]	IP13 [11]	IP13 [10]	IP13 [9]	IP13 [8]	IP13 [7]	IP13 [6]	IP13 [5]	IP13 [4]	IP13 [3]	IP13 [2]	IP13 [1]	IP13 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)
IP13[2:0]	SSI_WS2	HSCIF1_HCTS_N_B	SCIFA0_RXD_D	VI1_DATA3	Reserved	ATACS00_N	ETH_LINK_B	-
IP13[5:3]	SSI_SDATA2	HSCIF1_HRTS_N_B	SCIFA0_TXD_D	VI1_DATA4	Reserved	ATACS10_N	ETH_REFCLK_B	-
IP13[8:6]	SSI_SCK9	SCIF2_SCK_B	PWM2_B	VI1_DATA5	Reserved	EX_WAIT1	ETH_TXD1_B	-
IP13[11:9]	SSI_WS9	SCIF2_RXD_B	I2C3_SCL_E	VI1_DATA6	ATARD0_N	ETH_TX_EN_B	-	-
IP13[14:12]	SSI_SDATA9	SCIF2_TXD_B	I2C3_SDA_E	VI1_DATA7	ATADIR0_N	ETH_MAGIC_B	-	-
IP13[17:15]	AUDIO_CLKA	I2C0_SCL_B	SCIFA4_RXD_D	VI1_CLKENB	Reserved	Reserved	ETH_TXD0_B	-
IP13[20:18]	AUDIO_CLKB	I2C0_SDA_B	SCIFA4_TXD_D	VI1_FIELD	Reserved	Reserved	Reserved	ETH_MDC_B
IP13[23:21]	AUDIO_CLKC	I2C4_SCL_B	SCIFA5_RXD_D	VI1_HSYNC_N	Reserved	Reserved	Reserved	Reserved
IP13[26:24]	AUDIO_CLKOUT	I2C4_SDA_B	SCIFA5_TXD_D	VI1_VSYNC_N	Reserved	Reserved	Reserved	Reserved

Legend: - Setting prohibited

Table 5.2 shows the correspondence between the function signals and the bit settings in the GPIO/peripheral function select registers and peripheral function selecting registers.

Table 5.2 Correspondence between Function Signals and Register Bit Settings

GPIO	Peripheral-Module-(GP-Set-Value-=-1)								GPIO/ Peripheral	Peripheral
	Function-Selected-by-IP-Bits									
(GP-Set-Value-=-0)	Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	-Function-Selecting-Bit	-Function-Selecting-Bit
GP0[0]	D0	SCIFA3_SCK_B	IRQ4	-	-	-	-	-	GP0[0]	IP0[23:22]
GP0[1]	D1	SCIFA3_RXD_B	-	-	-	-	-	-	GP0[1]	IP0[24]
GP0[2]	D2	SCIFA3_TXD_B	-	-	-	-	-	-	GP0[2]	IP0[25]
GP0[3]	D3	I2C3_SCL_B	SCIF5_RXD_B	-	-	-	-	-	GP0[3]	IP0[27:26]
GP0[4]	D4	I2C3_SDA_B	SCIF5_TXD_B	-	-	-	-	-	GP0[4]	IP0[29:28]
GP0[5]	D5	SCIF4_RXD_B	I2C0_SCL_D	-	-	-	-	-	GP0[5]	IP0[31:30]
GP0[6]	D6	SCIF4_TXD_B	I2C0_SDA_D	-	-	-	-	-	GP0[6]	IP1[1:0]
GP0[7]	D7	IRQ3	TCLK1	PWM6_B	-	-	-	-	GP0[7]	IP1[3:2]
GP0[8]	D8	HSCIF2_HRX	I2C1_SCL_B	-	-	-	-	-	GP0[8]	IP1[5:4]
GP0[9]	D9	HSCIF2_HTX	I2C1_SDA_B	-	-	-	-	-	GP0[9]	IP1[7:6]
GP0[10]	D10	HSCIF2_HSCK	SCIF1_SCK_C	IRQ6	PWM5_C	-	-	-	GP0[10]	IP1[10:8]
GP0[11]	D11	HSCIF2_HCTS_N	SCIF1_RXD_C	I2C1_SCL_D	-	-	-	-	GP0[11]	IP1[12:11]
GP0[12]	D12	HSCIF2_HRTS_N	SCIF1_TXD_C	I2C1_SDA_D	-	-	-	-	GP0[12]	IP1[14:13]
GP0[13]	D13	SCIFA1_SCK	Reserved	PWM2_C	TCLK2_B	-	-	-	GP0[13]	IP1[17:15]
GP0[14]	D14	SCIFA1_RXD	I2C5_SCL_B	-	-	-	-	-	GP0[14]	IP1[19:18]
GP0[15]	D15	SCIFA1_TXD	I2C5_SDA_B	-	-	-	-	-	GP0[15]	IP1[21:20]
GP0[16]	A0	SCIFB1_SCK	PWM3_B	-	-	-	-	-	GP0[16]	IP1[23:22]
GP0[17]	A1	SCIFB1_TXD	-	-	-	-	-	-	GP0[17]	IP1[24]
GP0[18]	A2	-	-	-	-	-	-	-	GP0[18]	-
GP0[19]	A3	SCIFB0_SCK	-	-	-	-	-	-	GP0[19]	IP1[26]
GP0[20]	A4	SCIFB0_TXD	-	-	-	-	-	-	GP0[20]	IP1[27]
GP0[21]	A5	SCIFB0_RXD	PWM4_B	TPUTO3_C	-	-	-	-	GP0[21]	IP1[29:28]
GP0[22]	A6	SCIFB0_CTS_N	SCIFA4_RXD_B	TPUTO2_C	-	-	-	-	GP0[22]	IP1[31:30]
GP0[23]	A7	SCIFB0_RTS_N	SCIFA4_TXD_B	-	-	-	-	-	GP0[23]	IP2[1:0]
GP0[24]	A8	MSIOF1_RXD	SCIFA0_RXD_B	-	-	-	-	-	GP0[24]	IP2[3:2]
GP0[25]	A9	MSIOF1_TXD	SCIFA0_TXD_B	-	-	-	-	-	GP0[25]	IP2[5:4]
GP0[26]	A10	MSIOF1_SCK	IIC0_SCL_B	-	-	-	-	-	GP0[26]	IP2[7:6]
GP0[27]	A11	MSIOF1_SYNC	IIC0_SDA_B	-	-	-	-	-	GP0[27]	IP2[9:8]
GP0[28]	A12	MSIOF1_SS1	SCIFA5_RXD_B	-	-	-	-	-	GP0[28]	IP2[11:10]
GP0[29]	A13	MSIOF1_SS2	SCIFA5_TXD_B	-	-	-	-	-	GP0[29]	IP2[13:12]
GP0[30]	A14	MSIOF2_RXD	HSCIF0_HRX_B	DREQ1_N	-	-	-	-	GP0[30]	IP2[15:14]
GP0[31]	A15	MSIOF2_TXD	HSCIF0_HTX_B	DACK1	-	-	-	-	GP0[31]	IP2[17:16]
GP1[0]	A16	MSIOF2_SCK	HSCIF0_HSCK_B	Reserved	Reserved	CAN_CLK_C	TPUTO2_B	-	GP1[0]	IP2[20:18]
GP1[1]	A17	MSIOF2_SYNC	SCIF4_RXD_E	CAN1_RX_B	Reserved	-	-	-	GP1[1]	IP2[23:21]
GP1[2]	A18	MSIOF2_SS1	SCIF4_TXD_E	CAN1_TX_B	Reserved	-	-	-	GP1[2]	IP2[26:24]
GP1[3]	A19	MSIOF2_SS2	PWM4	TPUTO2	Reserved	-	-	-	GP1[3]	IP2[29:27]
GP1[4]	A20	SPCLK	Reserved	-	-	-	-	-	GP1[4]	IP2[31:30]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP1[5]	A21	MOSI_IO0	Reserved	-	-	-	-	-	GP1[5]	IP3[1:0]
GP1[6]	A22	MISO_IO1	Reserved	ATADIR1_N	-	-	-	-	GP1[6]	IP3[3:2]
GP1[7]	A23	IO2	Reserved	ATAWR1_N	-	-	-	-	GP1[7]	IP3[5:4]
GP1[8]	A24	IO3	EX_WAIT2	-	-	-	-	-	GP1[8]	IP3[7:6]
GP1[9]	A25	SSL	ATARD1_N	-	-	-	-	-	GP1[9]	IP3[9:8]
GP1[10]	CS0_N	VI1_DATA8	-	-	-	-	-	-	GP1[10]	IP3[10]
GP1[11]	CS1_N_A26	VI1_DATA9	-	-	-	-	-	-	GP1[11]	IP3[11]
GP1[12]	EX_CS0_N	VI1_DATA10	-	-	-	-	-	-	GP1[12]	IP3[12]
GP1[13]	EX_CS1_N	TPUTO3_B	SCIFB2_RXD	VI1_DATA11	-	-	-	-	GP1[13]	IP3[14:13]
GP1[14]	EX_CS2_N	PWM0	SCIF4_RXD_C	Reserved	Reserved	TPUTO3	SCIFB2_TXD	Reserved	GP1[14]	IP3[17:15]
GP1[15]	EX_CS3_N	SCIFA2_SCK	SCIF4_TXD_C	Reserved	Reserved	Reserved	SCIFB2_SCK	Reserved	GP1[15]	IP3[20:18]
GP1[16]	EX_CS4_N	SCIFA2_RXD	I2C2_SCL_E	Reserved	Reserved	Reserved	SCIFB2_CTS_N	Reserved	GP1[16]	IP3[23:21]
GP1[17]	EX_CS5_N	SCIFA2_TXD	I2C2_SDA_E	Reserved	Reserved	Reserved	SCIFB2_RTS_N	Reserved	GP1[17]	IP3[26:24]
GP1[18]	BS_N	DRACK0	PWM1_C	TPUTO0_C	ATACS01_N	Reserved	-	-	GP1[18]	IP3[29:27]
GP1[19]	RD_N	ATACS11_N	-	-	-	-	-	-	GP1[19]	IP3[30]
GP1[20]	RD_WR_N	ATAG1_N	-	-	-	-	-	-	GP1[20]	IP3[31]
GP1[21]	WE0_N	-	-	-	-	-	-	-	GP1[21]	-
GP1[22]	WE1_N	-	-	-	-	-	-	-	GP1[22]	-
GP1[23]	EX_WAIT0	CAN_CLK_B	SCIF_CLK	Reserved	-	-	-	-	GP1[23]	IP4[1:0]
GP1[24]	DREQ0_N	SCIFB1_RXD	-	-	-	-	-	-	GP1[24]	IP7[31]
GP1[25]	DACK0	-	-	-	-	-	-	-	GP1[25]	-
GP2[0]	DU0_DR0	Reserved	SCIF5_RXD_C	I2C2_SCL_D	Reserved	-	-	-	GP2[0]	IP4[4:2]
GP2[1]	DU0_DR1	Reserved	SCIF5_TXD_C	I2C2_SDA_D	Reserved	-	-	-	GP2[1]	IP4[7:5]
GP2[2]	DU0_DR2	Reserved	Reserved	-	-	-	-	-	GP2[2]	IP4[9:8]
GP2[3]	DU0_DR3	Reserved	Reserved	-	-	-	-	-	GP2[3]	IP4[11:10]
GP2[4]	DU0_DR4	Reserved	Reserved	-	-	-	-	-	GP2[4]	IP4[13:12]
GP2[5]	DU0_DR5	Reserved	Reserved	-	-	-	-	-	GP2[5]	IP4[15:14]
GP2[6]	DU0_DR6	Reserved	Reserved	-	-	-	-	-	GP2[6]	IP4[17:16]
GP2[7]	DU0_DR7	Reserved	Reserved	-	-	-	-	-	GP2[7]	IP4[19:18]
GP2[8]	DU0_DG0	Reserved	SCIFA0_RXD_C	I2C3_SCL_D	Reserved	-	-	-	GP2[8]	IP4[22:20]
GP2[9]	DU0_DG1	Reserved	SCIFA0_TXD_C	I2C3_SDA_D	Reserved	-	-	-	GP2[9]	IP4[25:23]
GP2[10]	DU0_DG2	Reserved	Reserved	-	-	-	-	-	GP2[10]	IP4[27:26]
GP2[11]	DU0_DG3	Reserved	Reserved	-	-	-	-	-	GP2[11]	IP4[29:28]
GP2[12]	DU0_DG4	Reserved	Reserved	-	-	-	-	-	GP2[12]	IP4[31:30]
GP2[13]	DU0_DG5	Reserved	Reserved	-	-	-	-	-	GP2[13]	IP5[1:0]
GP2[14]	DU0_DG6	Reserved	Reserved	-	-	-	-	-	GP2[14]	IP5[3:2]
GP2[15]	DU0_DG7	Reserved	Reserved	-	-	-	-	-	GP2[15]	IP5[5:4]
GP2[16]	DU0_DB0	Reserved	SCIFA4_RXD_C	I2C4_SCL_D	CAN0_RX_C	Reserved	-	-	GP2[16]	IP5[8:6]
GP2[17]	DU0_DB1	Reserved	SCIFA4_TXD_C	I2C4_SDA_D	CAN0_TX_C	Reserved	-	-	GP2[17]	IP5[11:9]
GP2[18]	DU0_DB2	Reserved	Reserved	-	-	-	-	-	GP2[18]	IP5[13:12]
GP2[19]	DU0_DB3	Reserved	Reserved	-	-	-	-	-	GP2[19]	IP5[15:14]
GP2[20]	DU0_DB4	Reserved	Reserved	-	-	-	-	-	GP2[20]	IP5[17:16]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP2[21]	DU0_DB5	Reserved	Reserved	-	-	-	-	-	GP2[21]	IP5[19:18]
GP2[22]	DU0_DB6	Reserved	Reserved	-	-	-	-	-	GP2[22]	IP5[21:20]
GP2[23]	DU0_DB7	Reserved	Reserved	-	-	-	-	-	GP2[23]	IP5[23:22]
GP2[24]	DU0_ DOTCLKIN	Reserved	Reserved	-	-	-	-	-	GP2[24]	IP5[25:24]
GP2[25]	DU0_DOTCLKOUT0	Reserved	Reserved	-	-	-	-	-	GP2[25]	IP5[27:26]
GP2[26]	DU0_DOTCLKOUT1	Reserved	Reserved	-	-	-	-	-	GP2[26]	IP5[29:28]
GP2[27]	DU0_ EXHSYNC_ DU0_HSYNC	Reserved	Reserved	-	-	-	-	-	GP2[27]	IP5[31:30]
GP2[28]	DU0_ EXVSYNC_ DU0_VSYNC	Reserved	Reserved	-	-	-	-	-	GP2[28]	IP6[1:0]
GP2[29]	DU0_EXODDF_ DU0_ODDF_DISP_CDE	Reserved	Reserved	-	-	-	-	-	GP2[29]	IP6[3:2]
GP2[30]	DU0_DISP	Reserved	Reserved	-	-	-	-	-	GP2[30]	IP6[5:4]
GP2[31]	DU0_CDE	Reserved	Reserved	-	-	-	-	-	GP2[31]	IP6[7:6]
GP3[0]	VI0_CLK	AVB_RX_CLK	-	-	-	-	-	-	GP3[0]	IP6[8]
GP3[1]	VI0_DATA0_VI0_B0	AVB_RX_DV	-	-	-	-	-	-	GP3[1]	IP6[9]
GP3[2]	VI0_DATA1_VI0_B1	AVB_RXD0	-	-	-	-	-	-	GP3[2]	IP6[10]
GP3[3]	VI0_DATA2_VI0_B2	AVB_RXD1	-	-	-	-	-	-	GP3[3]	IP6[11]
GP3[4]	VI0_DATA3_VI0_B3	AVB_RXD2	-	-	-	-	-	-	GP3[4]	IP6[12]
GP3[5]	VI0_DATA4_VI0_B4	AVB_RXD3	-	-	-	-	-	-	GP3[5]	IP6[13]
GP3[6]	VI0_DATA5_VI0_B5	AVB_RXD4	-	-	-	-	-	-	GP3[6]	IP6[14]
GP3[7]	VI0_DATA6_VI0_B6	AVB_RXD5	-	-	-	-	-	-	GP3[7]	IP6[15]
GP3[8]	VI0_DATA7_VI0_B7	AVB_RXD6	-	-	-	-	-	-	GP3[8]	IP6[16]
GP3[9]	VI0_CLKENB	I2C3_SCL	SCIFA5_RXD_C	Reserved	AVB_RXD7	-	-	-	GP3[9]	IP6[19:17]
GP3[10]	VI0_FIELD	I2C3_SDA	SCIFA5_TXD_C	Reserved	AVB_RX_ER	-	-	-	GP3[10]	IP6[22:20]
GP3[11]	VI0_HSYNC_N	SCIF0_RXD_B	I2C0_SCL_C	Reserved	AVB_COL	-	-	-	GP3[11]	IP6[25:23]
GP3[12]	VI0_VSYNC_N	SCIF0_TXD_B	I2C0_SDA_C	AUDIO_CLKOUT_B	AVB_TX_EN	-	-	-	GP3[12]	IP6[28:26]
GP3[13]	ETH_MDIO	VI0_G0	MSIOF2_RXD_B	I2C5_SCL_D	AVB_TX_CLK	Reserved	Reserved	-	GP3[13]	IP6[31:29]
GP3[14]	ETH_CRS_DV	VI0_G1	MSIOF2_TXD_B	I2C5_SDA_D	AVB_TXD0	Reserved	Reserved	-	GP3[14]	IP7[2:0]
GP3[15]	ETH_RX_ER	VI0_G2	MSIOF2_SCK_B	CAN0_RX_B	AVB_TXD1	Reserved	Reserved	-	GP3[15]	IP7[5:3]
GP3[16]	ETH_RXD0	VI0_G3	MSIOF2_SYNC_B	CAN0_TX_B	AVB_TXD2	Reserved	Reserved	-	GP3[16]	IP7[8:6]
GP3[17]	ETH_RXD1	VI0_G4	MSIOF2_SS1_B	SCIF4_RXD_D	AVB_TXD3	Reserved	-	-	GP3[17]	IP7[11:9]
GP3[18]	ETH_LINK	VI0_G5	MSIOF2_SS2_B	SCIF4_TXD_D	AVB_TXD4	Reserved	-	-	GP3[18]	IP7[14:12]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP3[19]	ETH_REF_CLK	VI0_G6	SCIF2_SCK_C	AVB_TXD5	SSI_SCK5_B	-	-	-	GP3[19]	IP7[17:15]
GP3[20]	ETH_TXD1	VI0_G7	SCIF2_RXD_C	IIC0_SCL_D	AVB_TXD6	SSI_WS5_B	-	-	GP3[20]	IP7[20:18]
GP3[21]	ETH_TX_EN	VI0_R0	SCIF2_TXD_C	IIC0_SDA_D	AVB_TXD7	SSI_SDATA5_B	-	-	GP3[21]	IP7[23:21]
GP3[22]	ETH_MAGIC	VI0_R1	SCIF3_SCK_B	AVB_TX_ER	SSI_SCK6_B	-	-	-	GP3[22]	IP7[26:24]
GP3[23]	ETH_TXD0	VI0_R2	SCIF3_RXD_B	I2C4_SCL_E	AVB_GTX_CLK	SSI_WS6_B	-	-	GP3[23]	IP7[29:27]
GP3[24]	ETH_MDC	VI0_R3	SCIF3_TXD_B	I2C4_SDA_E	AVB_MDC	SSI_SDATA6_B	-	-	GP3[24]	IP8[2:0]
GP3[25]	HSCIF0_HRX	VI0_R4	I2C1_SCL_C	AUDIO_CLKA_B	AVB_MDIO	SSI_SCK78_B	-	-	GP3[25]	IP8[5:3]
GP3[26]	HSCIF0_HTX	VI0_R5	I2C1_SDA_C	AUDIO_CLKB_B	AVB_LINK	SSI_WS78_B	-	-	GP3[26]	IP8[8:6]
GP3[27]	HSCIF0_HCTS_N	VI0_R6	SCIF0_RXD_D	I2C0_SCL_E	AVB_MAGIC	SSI_SDATA7_B	-	-	GP3[27]	IP8[11:9]
GP3[28]	HSCIF0_HRTS_N	VI0_R7	SCIF0_TXD_D	I2C0_SDA_E	AVB_PHY_INT	SSI_SDATA8_B	-	-	GP3[28]	IP8[14:12]
GP3[29]	HSCIF0_HSCK	SCIF_CLK_B	AVB_CRS	AUDIO_CLKC_B	-	-	-	-	GP3[29]	IP8[16:15]
GP3[30]	I2C0_SCL	SCIF0_RXD_C	PWM5	TCLK1_B	AVB_GTXREFCLK	CAN1_RX_D	TPUTO0_B	-	GP3[30]	IP8[19:17]
GP3[31]	I2C0_SDA	SCIF0_TXD_C	TPUTO0	CAN_CLK	DVC_MUTE	CAN1_TX_D	-	-	GP3[31]	IP8[22:20]
GP4[0]	I2C1_SCL	SCIF4_RXD	PWM5_B	DU1_DR0	Reserved	Reserved	TPUTO1_B	-	GP4[0]	IP8[25:23]
GP4[1]	I2C1_SDA	SCIF4_TXD	IRQ5	DU1_DR1	Reserved	Reserved	Reserved	-	GP4[1]	IP8[28:26]
GP4[2]	MSIOF0_RXD	SCIF5_RXD	I2C2_SCL_C	DU1_DR2	Reserved	Reserved	Reserved	Reserved	GP4[2]	IP8[31:29]
GP4[3]	MSIOF0_TXD	SCIF5_TXD	I2C2_SDA_C	DU1_DR3	Reserved	Reserved	Reserved	Reserved	GP4[3]	IP9[2:0]
GP4[4]	MSIOF0_SCK	IRQ0	Reserved	DU1_DR4	Reserved	TPUTO1_C	-	-	GP4[4]	IP9[5:3]
GP4[5]	MSIOF0_SYNC	PWM1	Reserved	DU1_DR5	Reserved	Reserved	-	-	GP4[5]	IP9[8:6]
GP4[6]	MSIOF0_SS1	SCIFA0_RXD	Reserved	DU1_DR6	Reserved	Reserved	Reserved	-	GP4[6]	IP9[11:9]
GP4[7]	MSIOF0_SS2	SCIFA0_TXD	Reserved	DU1_DR7	Reserved	Reserved	Reserved	-	GP4[7]	IP9[14:12]
GP4[8]	HSCIF1_HRX	I2C4_SCL	PWM6	DU1_DG0	-	-	-	-	GP4[8]	IP9[16:15]
GP4[9]	HSCIF1_HTX	I2C4_SDA	TPUTO1	DU1_DG1	-	-	-	-	GP4[9]	IP9[18:17]
GP4[10]	HSCIF1_HSCK	PWM2	Reserved	DU1_DG2	Reserved	Reserved	Reserved	-	GP4[10]	IP9[21:19]
GP4[11]	HSCIF1_HCTS_N	SCIFA4_RXD	Reserved	DU1_DG3	SSI_SCK1_B	Reserved	Reserved	-	GP4[11]	IP9[24:22]
GP4[12]	HSCIF1_HRTS_N	SCIFA4_TXD	Reserved	DU1_DG4	SSI_WS1_B	Reserved	Reserved	-	GP4[12]	IP9[27:25]
GP4[13]	SCIF1_SCK	PWM3	TCLK2	DU1_DG5	SSI_SDATA1_B	Reserved	Reserved	-	GP4[13]	IP9[30:28]
GP4[14]	SCIF1_RXD	I2C5_SCL	DU1_DG6	SSI_SCK2_B	Reserved	Reserved	-	-	GP4[14]	IP10[2:0]
GP4[15]	SCIF1_TXD	I2C5_SDA	DU1_DG7	SSI_WS2_B	Reserved	Reserved	-	-	GP4[15]	IP10[5:3]
GP4[16]	SCIF2_RXD	IIC0_SCL	DU1_DB0	SSI_SDATA2_B	Reserved	Reserved	Reserved	-	GP4[16]	IP10[8:6]
GP4[17]	SCIF2_TXD	IIC0_SDA	DU1_DB1	SSI_SCK9_B	Reserved	Reserved	Reserved	-	GP4[17]	IP10[11:9]
GP4[18]	SCIF2_SCK	IRQ1	DU1_DB2	SSI_WS9_B	Reserved	Reserved	Reserved	-	GP4[18]	IP10[14:12]
GP4[19]	SCIF3_SCK	IRQ2	Reserved	DU1_DB3	SSI_SDATA9_B	Reserved	Reserved	Reserved	GP4[19]	IP10[17:15]
GP4[20]	SCIF3_RXD	I2C1_SCL_E	Reserved	DU1_DB4	AUDIO_CLKA_C	SSI_SCK4_B	Reserved	Reserved	GP4[20]	IP10[20:18]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral-Function-Selecting-Bit	Peripheral-Function-Selecting-Bit
GP4[21]	SCIF3_TXD	I2C1_SDA_E	Reserved	DU1_DB5	AUDIO_CLKB_C	SSI_WS4_B	Reserved	Reserved	GP4[21]	IP10[23:21]
GP4[22]	I2C2_SCL	SCIFA5_RXD	DU1_DB6	AUDIO_CLKC_C	SSI_SDATA4_B	Reserved	-	-	GP4[22]	IP10[26:24]
GP4[23]	I2C2_SDA	SCIFA5_TXD	DU1_DB7	AUDIO_CLKOUT_C	Reserved	-	-	-	GP4[23]	IP10[29:27]
GP4[24]	SSI_SCK5	SCIFA3_SCK	DU1_DOTCLKIN	Reserved	-	-	-	-	GP4[24]	IP10[31:30]
GP4[25]	SSI_WS5	SCIFA3_RXD	I2C3_SCL_C	DU1_DOTCLKOUT0	Reserved	-	-	-	GP4[25]	IP11[2:0]
GP4[26]	SSI_SDATA5	SCIFA3_TXD	I2C3_SDA_C	DU1_DOTCLKOUT1	Reserved	-	-	-	GP4[26]	IP11[5:3]
GP4[27]	SSI_SCK6	SCIFA1_SCK_B	DU1_EXHSYNC_DU1_HSYNC	Reserved	-	-	-	-	GP4[27]	IP11[7:6]
GP4[28]	SSI_WS6	SCIFA1_RXD_B	I2C4_SCL_C	DU1_EXVSYNC_DU1_VSYNC	Reserved	-	-	-	GP4[28]	IP11[10:8]
GP4[29]	SSI_SDATA6	SCIFA1_TXD_B	I2C4_SDA_C	DU1_EXODDF_DU1_ODDF_DISP_CDE	Reserved	-	-	-	GP4[29]	IP11[13:11]
GP4[30]	SSI_SCK78	SCIFA2_SCK_B	I2C5_SDA_C	DU1_DISP	-	-	-	-	GP4[30]	IP11[15:14]
GP4[31]	SSI_WS78	SCIFA2_RXD_B	I2C5_SCL_C	DU1_CDE	-	-	-	-	GP4[31]	IP11[17:16]
GP5[0]	SSI_SDATA7	SCIFA2_TXD_B	IRQ8	AUDIO_CLKA_D	CAN_CLK_D	Reserved	-	-	GP5[0]	IP11[20:18]
GP5[1]	SSI_SCK0129	MSIOF1_RXD_B	SCIF5_RXD_D	Reserved	Reserved	Reserved	-	-	GP5[1]	IP11[23:21]
GP5[2]	SSI_WS0129	MSIOF1_TXD_B	SCIF5_TXD_D	Reserved	Reserved	-	-	-	GP5[2]	IP11[26:24]
GP5[3]	SSI_SDATA0	MSIOF1_SCK_B	PWM0_B	Reserved	Reserved	-	-	-	GP5[3]	IP11[29:27]
GP5[4]	SSI_SCK34	MSIOF1_SYNC_B	SCIFA1_SCK_C	Reserved	Reserved	DREQ1_N_B	-	-	GP5[4]	IP12[2:0]
GP5[5]	SSI_WS34	MSIOF1_SS1_B	SCIFA1_RXD_C	Reserved	CAN1_RX_C	DACK1_B	-	-	GP5[5]	IP12[5:3]
GP5[6]	SSI_SDATA3	MSIOF1_SS2_B	SCIFA1_TXD_C	Reserved	CAN1_TX_C	DREQ2_N	-	-	GP5[6]	IP12[8:6]
GP5[7]	SSI_SCK4	Reserved	Reserved	Reserved	-	-	-	-	GP5[7]	IP12[10:9]
GP5[8]	SSI_WS4	Reserved	Reserved	Reserved	-	-	-	-	GP5[8]	IP12[12:11]
GP5[9]	SSI_SDATA4	Reserved	Reserved	Reserved	-	-	-	-	GP5[9]	IP12[14:13]
GP5[10]	SSI_SDATA8	SCIF1_SCK_B	PWM1_B	IRQ9	Reserved	DACK2	ETH_MDIO_B	-	GP5[10]	IP12[17:15]
GP5[11]	SSI_SCK1	SCIF1_RXD_B	IIC0_SCL_C	VI1_CLK	CAN0_RX_D	AVB_AVTP_CAPTURE	ETH_CRS_DV_B	-	GP5[11]	IP12[20:18]
GP5[12]	SSI_WS1	SCIF1_TXD_B	IIC0_SDA_C	VI1_DATA0	CAN0_TX_D	AVB_AVTP_MATCH	ETH_RX_ER_B	-	GP5[12]	IP12[23:21]
GP5[13]	SSI_SDATA1	HSCIF1_HRX_B	VI1_DATA1	Reserved	ATAWR0_N	ETH_RXD0_B	-	-	GP5[13]	IP12[26:24]
GP5[14]	SSI_SCK2	HSCIF1_HTX_B	VI1_DATA2	Reserved	ATAG0_N	ETH_RXD1_B	-	-	GP5[14]	IP12[29:27]
GP5[15]	SSI_WS2	HSCIF1_HCTS_N_B	SCIFA0_RXD_D	VI1_DATA3	Reserved	ATACS00_N	ETH_LINK_B	-	GP5[15]	IP13[2:0]
GP5[16]	SSI_SDATA2	HSCIF1_HRTS_N_B	SCIFA0_TXD_D	VI1_DATA4	Reserved	ATACS10_N	ETH_REF_CLK_B	-	GP5[16]	IP13[5:3]
GP5[17]	SSI_SCK9	SCIF2_SCK_B	PWM2_B	VI1_DATA5	Reserved	EX_WAIT1	ETH_TXD1_B	-	GP5[17]	IP13[8:6]
GP5[18]	SSI_WS9	SCIF2_RXD_B	I2C3_SCL_E	VI1_DATA6	ATARD0_N	ETH_TX_EN_B	-	-	GP5[18]	IP13[11:9]
GP5[19]	SSI_SDATA9	SCIF2_TXD_B	I2C3_SDA_E	VI1_DATA7	ATADIR0_N	ETH_MAGIC_B	-	-	GP5[19]	IP13[14:12]
GP5[20]	AUDIO_CLKA	I2C0_SCL_B	SCIFA4_RXD_D	VI1_CLKENB	Reserved	Reserved	ETH_TXD0_B	-	GP5[20]	IP13[17:15]
GP5[21]	AUDIO_CLKB	I2C0_SDA_B	SCIFA4_TXD_D	VI1_FIELD	Reserved	Reserved	Reserved	ETH_MDC_B	GP5[21]	IP13[20:18]
GP5[22]	AUDIO_CLKC	I2C4_SCL_B	SCIFA5_RXD_D	VI1_HSYNC_N	Reserved	Reserved	Reserved	Reserved	GP5[22]	IP13[23:21]

GPIO (GP-Set-Value-=-0)	Peripheral-Module-(GP-Set-Value-=-1) Function-Selected-by-IP-Bits Function-1 (IP-Set-Value-=-0)	Function-2 (IP-Set-Value-=-1)	Function-3 (IP-Set-Value-=-2)	Function-4 (IP-Set-Value-=-3)	Function-5 (IP-Set-Value-=-4)	Function-6 (IP-Set-Value-=-5)	Function-7 (IP-Set-Value-=-6)	Function-8 (IP-Set-Value-=-7)	GPIO/ Peripheral -Function- Selecting- Bit	Peripheral- Function- Selecting- Bit
GP5[23]	AUDIO_CLKOUT	I2C4_SDA_B	SCIFA5_TXD_D	VI1_VSYNC_N	Reserved	Reserved	Reserved	Reserved	GP5[23]	IP13[26:24]
GP5[24]	USB0_PWEN	-	-	-	-	-	-	-	GP5[24]	-
GP5[25]	USB0_OVC	-	-	-	-	-	-	-	GP5[25]	-
GP5[26]	USB1_PWEN	-	-	-	-	-	-	-	GP5[26]	-
GP5[27]	USB1_OVC	-	-	-	-	-	-	-	GP5[27]	-
GP6[0]	SD0_CLK	-	-	-	-	-	-	-	GP6[0]	-
GP6[1]	SD0_CMD	-	-	-	-	-	-	-	GP6[1]	-
GP6[2]	SD0_DATA0	-	-	-	-	-	-	-	GP6[2]	-
GP6[3]	SD0_DATA1	-	-	-	-	-	-	-	GP6[3]	-
GP6[4]	SD0_DATA2	-	-	-	-	-	-	-	GP6[4]	-
GP6[5]	SD0_DATA3	-	-	-	-	-	-	-	GP6[5]	-
GP6[6]	SD0_CD	-	-	-	-	-	-	-	GP6[6]	-
GP6[7]	SD0_WP	-	-	-	-	-	-	-	GP6[7]	-
GP6[8]	SD1_CLK	-	-	-	-	-	-	-	GP6[8]	-
GP6[9]	SD1_CMD	-	-	-	-	-	-	-	GP6[9]	-
GP6[10]	SD1_DATA0	-	-	-	-	-	-	-	GP6[10]	-
GP6[11]	SD1_DATA1	-	-	-	-	-	-	-	GP6[11]	-
GP6[12]	SD1_DATA2	-	-	-	-	-	-	-	GP6[12]	-
GP6[13]	SD1_DATA3	-	-	-	-	-	-	-	GP6[13]	-
GP6[14]	SD1_CD	CAN0_RX	-	-	-	-	-	-	GP6[14]	IP0[0]
GP6[15]	SD1_WP	IRQ7	CAN0_TX	-	-	-	-	-	GP6[15]	IP0[9:8]
GP6[16]	MMC_CLK	SD2_CLK	-	-	-	-	-	-	GP6[16]	IP0[10]
GP6[17]	MMC_CMD	SD2_CMD	-	-	-	-	-	-	GP6[17]	IP0[11]
GP6[18]	MMC_D0	SD2_DATA0	-	-	-	-	-	-	GP6[18]	IP0[12]
GP6[19]	MMC_D1	SD2_DATA1	-	-	-	-	-	-	GP6[19]	IP0[13]
GP6[20]	MMC_D2	SD2_DATA2	-	-	-	-	-	-	GP6[20]	IP0[14]
GP6[21]	MMC_D3	SD2_DATA3	-	-	-	-	-	-	GP6[21]	IP0[15]
GP6[22]	MMC_D4	SD2_CD	-	-	-	-	-	-	GP6[22]	IP0[16]
GP6[23]	MMC_D5	SD2_WP	-	-	-	-	-	-	GP6[23]	IP0[17]
GP6[24]	MMC_D6	SCIF0_RXD	I2C2_SCL_B	CAN1_RX	-	-	-	-	GP6[24]	IP0[19:18]
GP6[25]	MMC_D7	SCIF0_TXD	I2C2_SDA_B	CAN1_TX	-	-	-	-	GP6[25]	IP0[21:20]

Legend: - Setting prohibited

5.3.23 Module Select Register (MOD_SEL)

Function: MOD_SEL selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the ADG, ADI, CAN, DR, I2C and AVB an is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups. When ssi7 and ssi8 (in MOD_SEL3 register) are to be used simultaneously, the values of sel_ssi7[0] and sel_ssi8[0] must be the same so that the selected pins belong to the same group. If this is not the case, correct operation is not guaranteed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_adg [1]	sel_adg [0]	—	sel_can [1]	sel_can [0]	—	—	—	—	—	—	—	sel_eth [0]	—	sel_i2c 00[2]	sel_i2c 00[1]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_i2c 00[0]	sel_i2c 01[2]	sel_i2c 01[1]	sel_i2c 01[0]	sel_i2c 02[2]	sel_i2c 02[1]	sel_i2c 02[0]	sel_i2c 03[2]	sel_i2c 03[1]	sel_i2c 03[0]	sel_i2c 04[2]	sel_i2c 04[1]	sel_i2c 04[0]	sel_i2c 05[1]	sel_i2c 05[0]	sel_avb [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_adg[1:0]	+ select pin AUDIO_CLKA for function AUDIO_CLKA + select pin AUDIO_CLKB for function AUDIO_CLKB + select pin AUDIO_CLKC for function AUDIO_CLKC + select pin AUDIO_CLKOUT for function AUDIO_CLKOUT	+ select pin HSCIF0_HRX for function AUDIO_CLKA_B + select pin HSCIF0_HSCK for function AUDIO_CLKC_B + select pin HSCIF0_HTX for function AUDIO_CLKB_B + select pin VI0_VSYNC_N for function AUDIO_CLKOUT_B	+ select pin I2C2_SCL for function AUDIO_CLKC_C + select pin I2C2_SDA for function AUDIO_CLKOUT_C + select pin SCIF3_RXD for function AUDIO_CLKA_C + select pin SCIF3_TXD for function AUDIO_CLKB_C	+ select pin SSI_SDATA7 for function AUDIO_CLKA_D	
sel_can[1:0]	+ select pin I2C0_SDA for function CAN_CLK	+ select pin EX_WAIT0 for function CAN_CLK_B	+ select pin A16 for function CAN_CLK_C	+ select pin SSI_SDATA7 for function CAN_CLK_D	

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_eth[0]	+ select pin ETH_CRS_DV for function ETH_CRS_DV + select pin ETH_LINK for function ETH_LINK + select pin ETH_MAGIC for function ETH_MAGIC + select pin ETH_MDC for function ETH_MDC + select pin ETH_MDIO for function ETH_MDIO + select pin ETH_REF_CLK for function ETH_REF_CLK + select pin ETH_RXD0 for function ETH_RXD0 + select pin ETH_RXD1 for function ETH_RXD1 + select pin ETH_RX_ER for function ETH_RX_ER + select pin ETH_TXD0 for function ETH_TXD0 + select pin ETH_TXD1 for function ETH_TXD1 + select pin ETH_TX_EN for function ETH_TX_EN	+ select pin AUDIO_CLKA for function ETH_TXD0_B + select pin AUDIO_CLKB for function ETH_MDC_B + select pin SSI_SCK1 for function ETH_CRS_DV_B + select pin SSI_SCK2 for function ETH_RXD1_B + select pin SSI_SCK9 for function ETH_TXD1_B + select pin SSI_SDATA1 for function ETH_RXD0_B + select pin SSI_SDATA2 for function ETH_REF_CLK_B + select pin SSI_SDATA8 for function ETH_MDIO_B + select pin SSI_SDATA9 for function ETH_MAGIC_B + select pin SSI_WS1 for function ETH_RX_ER_B + select pin SSI_WS2 for function ETH_LINK_B + select pin SSI_WS9 for function ETH_TX_EN_B			
sel_i2c00[2:0]	+ select pin I2C0_SCL for function I2C0_SCL + select pin I2C0_SDA for function I2C0_SDA	+ select pin AUDIO_CLKA for function I2C0_SCL_B + select pin AUDIO_CLKB for function I2C0_SDA_B	+ select pin VI0_HSYNC_N for function I2C0_SCL_C + select pin VI0_VSYNC_N for function I2C0_SDA_C	+ select pin D5 for function I2C0_SCL_D + select pin D6 for function I2C0_SDA_D	+ select pin HSCIF0_HCTS_N for function I2C0_SCL_E + select pin HSCIF0_HRTS_N for function I2C0_SDA_E
sel_i2c01[2:0]	+ select pin I2C1_SCL for function I2C1_SCL + select pin I2C1_SDA for function I2C1_SDA	+ select pin D8 for function I2C1_SCL_B + select pin D9 for function I2C1_SDA_B	+ select pin HSCIF0_HRX for function I2C1_SCL_C + select pin HSCIF0_HTX for function I2C1_SDA_C	+ select pin D11 for function I2C1_SCL_D + select pin D12 for function I2C1_SDA_D	+ select pin SCIF3_RXD for function I2C1_SCL_E + select pin SCIF3_TXD for function I2C1_SDA_E
sel_i2c02[2:0]	+ select pin I2C2_SCL for function I2C2_SCL + select pin I2C2_SDA for function I2C2_SDA	+ select pin MMC_D6 for function I2C2_SCL_B + select pin MMC_D7 for function I2C2_SDA_B	+ select pin MSIOF0_RXD for function I2C2_SCL_C + select pin MSIOF0_TXD for function I2C2_SDA_C	+ select pin DU0_DR0 for function I2C2_SCL_D + select pin DU0_DR1 for function I2C2_SDA_D	+ select pin EX_CS4_N for function I2C2_SCL_E + select pin EX_CS5_N for function I2C2_SDA_E
sel_i2c03[2:0]	+ select pin VI0_CLKENB for function I2C3_SCL + select pin VI0_FIELD for function I2C3_SDA	+ select pin D3 for function I2C3_SCL_B + select pin D4 for function I2C3_SDA_B	+ select pin SSI_SDATA5 for function I2C3_SDA_C + select pin SSI_WS5 for function I2C3_SCL_C	+ select pin DU0_DG0 for function I2C3_SCL_D + select pin DU0_DG1 for function I2C3_SDA_D	+ select pin SSI_SDATA9 for function I2C3_SDA_E + select pin SSI_WS9 for function I2C3_SCL_E
sel_i2c04[2:0]	+ select pin HSCIF1_HRX for function I2C4_SCL + select pin HSCIF1_HTX for function I2C4_SDA	+ select pin AUDIO_CLKC for function I2C4_SCL_B + select pin AUDIO_CLKOUT for function I2C4_SDA_B	+ select pin SSI_SDATA6 for function I2C4_SDA_C + select pin SSI_WS6 for function I2C4_SCL_C	+ select pin DU0_DB0 for function I2C4_SCL_D + select pin DU0_DB1 for function I2C4_SDA_D	+ select pin ETH_MDC for function I2C4_SDA_E + select pin ETH_TXD0 for function I2C4_SCL_E
sel_i2c05[1:0]	+ select pin SCIF1_RXD for function I2C5_SCL + select pin SCIF1_TXD for function I2C5_SDA	+ select pin D14 for function I2C5_SCL_B + select pin D15 for function I2C5_SDA_B	+ select pin SSI_SCK78 for function I2C5_SDA_C + select pin SSI_WS78 for function I2C5_SCL_C	+ select pin ETH_CRS_DV for function I2C5_SDA_D + select pin ETH_MDIO for function I2C5_SCL_D	

Legend: – Setting prohibited

5.3.24 Module Select Register 2 (MOD_SEL2)

Function: MOD_SEL2 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the IIC, LBS, MSI, RAD, SCIF, TMU, CAN and HSCIF is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. When ssi8 and ssi7 (in MOD_SEL3 register) are to be used simultaneously, the values of sel_ssi8[0] and sel_ssi7[0] must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	sel_iic0[1]	sel_iic0[0]	sel_lbs[0]	sel_msi1[0]	sel_msi2[0]	sel_rad[0]	—	—	sel_scifa0[1]	sel_scifa0[0]	sel_scifa1[1]	sel_scifa1[0]	sel_scifa2[0]	sel_scifa3[0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_scifa4[1]	sel_scifa4[0]	sel_scifa5[1]	sel_scifa5[0]	—	sel_tmu[0]	—	—	sel_can0[1]	sel_can0[0]	sel_can1[1]	sel_can1[0]	sel_hscif0[0]	sel_hscif1[0]	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_iic0[1:0]	+ select pin SCIF2_RXD for function IIC0_SCL + select pin SCIF2_TXD for function IIC0_SDA	+ select pin A10 for function IIC0_SCL_B + select pin A11 for function IIC0_SDA_B	+ select pin SSI_SCK1 for function IIC0_SCL_C + select pin SSI_WS1 for function IIC0_SDA_C	+ select pin ETH_TXD1 for function IIC0_SCL_D + select pin ETH_TX_EN for function IIC0_SDA_D	
sel_lbs[0]	+ select pin A14 for function DREQ1_N + select pin A15 for function DACK1	+ select pin SSI_SCK34 for function DREQ1_N_B + select pin SSI_WS34 for function DACK1_B			
sel_msi1[0]	+ select pin A10 for function MSIOF1_SCK + select pin A11 for function MSIOF1_SYNC + select pin A12 for function MSIOF1_SS1 + select pin A13 for function MSIOF1_SS2 + select pin A8 for function MSIOF1_RXD + select pin A9 for function MSIOF1_TXD	+ select pin SSI_SCK0129 for function MSIOF1_RXD_B + select pin SSI_SCK34 for function MSIOF1_SYNC_B + select pin SSI_SDATA0 for function MSIOF1_SCK_B + select pin SSI_SDATA3 for function MSIOF1_SS2_B + select pin SSI_WS0129 for function MSIOF1_TXD_B + select pin SSI_WS34 for function MSIOF1_SS1_B			

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_msi2[0]	+ select pin A14 for function MSIOF2_RXD + select pin A15 for function MSIOF2_TXD + select pin A16 for function MSIOF2_SCK + select pin A17 for function MSIOF2_SYNC + select pin A18 for function MSIOF2_SS1 + select pin A19 for function MSIOF2_SS2	+ select pin ETH_CRS_DV for function MSIOF2_TXD_B + select pin ETH_LINK for function MSIOF2_SS2_B + select pin ETH_MDIO for function MSIOF2_RXD_B + select pin ETH_RXD0 for function MSIOF2_SYNC_B + select pin ETH_RXD1 for function MSIOF2_SS1_B + select pin ETH_RX_ER for function MSIOF2_SCK_B			
sel_rad[0]	+ select pin ETH_CRS_DV for function ADICS_SAMP + select pin ETH_LINK for function ADICHS2 + select pin ETH_MDIO for function ADIDATA + select pin ETH_RXD0 for function ADICHS0 + select pin ETH_RXD1 for function ADICHS1 + select pin ETH_RX_ER for function ADICLK	+ select pin SSI_SCK0129 for function ADIDATA_B + select pin SSI_SCK34 for function ADICHS0_B + select pin SSI_SDATA0 for function ADICLK_B + select pin SSI_SDATA3 for function ADICHS2_B + select pin SSI_WS0129 for function ADICS_SAMP_B + select pin SSI_WS34 for function ADICHS1_B			
sel_scifa0[1:0]	+ select pin MSIOF0_SS1 for function SCIFA0_RXD + select pin MSIOF0_SS2 for function SCIFA0_TXD	+ select pin A8 for function SCIFA0_RXD_B + select pin A9 for function SCIFA0_TXD_B	+ select pin DU0_DG0 for function SCIFA0_RXD_C + select pin DU0_DG1 for function SCIFA0_TXD_C	+ select pin SSI_SDATA2 for function SCIFA0_TXD_D + select pin SSI_WS2 for function SCIFA0_RXD_D	
sel_scifa1[1:0]	+ select pin D13 for function SCIFA1_SCK + select pin D14 for function SCIFA1_RXD + select pin D15 for function SCIFA1_TXD	+ select pin SSI_SCK6 for function SCIFA1_SCK_B + select pin SSI_SDATA6 for function SCIFA1_TXD_B + select pin SSI_WS6 for function SCIFA1_RXD_B	+ select pin SSI_SCK34 for function SCIFA1_SCK_C + select pin SSI_SDATA3 for function SCIFA1_TXD_C + select pin SSI_WS34 for function SCIFA1_RXD_C		
sel_scifa2[0]	+ select pin EX_CS3_N for function SCIFA2_SCK + select pin EX_CS4_N for function SCIFA2_RXD + select pin EX_CS5_N for function SCIFA2_TXD	+ select pin SSI_SCK78 for function SCIFA2_SCK_B + select pin SSI_SDATA7 for function SCIFA2_TXD_B + select pin SSI_WS78 for function SCIFA2_RXD_B			
sel_scifa3[0]	+ select pin SSI_SCK5 for function SCIFA3_SCK + select pin SSI_SDATA5 for function SCIFA3_TXD + select pin SSI_WS5 for function SCIFA3_RXD	+ select pin D0 for function SCIFA3_SCK_B + select pin D1 for function SCIFA3_RXD_B + select pin D2 for function SCIFA3_TXD_B			
sel_scifa4[1:0]	+ select pin HSCIF1_HCTS_N for function SCIFA4_RXD + select pin HSCIF1_HRTS_N for function SCIFA4_TXD	+ select pin A6 for function SCIFA4_RXD_B + select pin A7 for function SCIFA4_TXD_B	+ select pin DU0_DB0 for function SCIFA4_RXD_C + select pin DU0_DB1 for function SCIFA4_TXD_C	+ select pin AUDIO_CLKA for function SCIFA4_RXD_D + select pin AUDIO_CLKB for function SCIFA4_TXD_D	
sel_scifa5[1:0]	+ select pin I2C2_SCL for function SCIFA5_RXD + select pin I2C2_SDA for function SCIFA5_TXD	+ select pin A12 for function SCIFA5_RXD_B + select pin A13 for function SCIFA5_TXD_B	+ select pin VI0_CLKENB for function SCIFA5_RXD_C + select pin VI0_FIELD for function SCIFA5_TXD_C	+ select pin AUDIO_CLKC for function SCIFA5_RXD_D + select pin AUDIO_CLKOUT for function SCIFA5_TXD_D	
sel_tmu[0]	+ select pin D7 for function TCLK1 + select pin SCIF1_SCK for function TCLK2	+ select pin D13 for function TCLK2_B + select pin I2C0_SCL for function TCLK1_B			
sel_can0[1:0]	+ select pin SD1_CD for function CAN0_RX + select pin SD1_WP for function CAN0_TX	+ select pin ETH_RXD0 for function CAN0_TX_B + select pin ETH_RX_ER for function CAN0_RX_B	+ select pin DU0_DB0 for function CAN0_RX_C + select pin DU0_DB1 for function CAN0_TX_C	+ select pin SSI_SCK1 for function CAN0_RX_D + select pin SSI_WS1 for function CAN0_TX_D	
sel_can1[1:0]	+ select pin MMC_D6 for function CAN1_RX + select pin MMC_D7 for function CAN1_TX	+ select pin A17 for function CAN1_RX_B + select pin A18 for function CAN1_TX_B	+ select pin SSI_SDATA3 for function CAN1_TX_C + select pin SSI_WS34 for function CAN1_RX_C	+ select pin I2C0_SCL for function CAN1_RX_D + select pin I2C0_SDA for function CAN1_TX_D	
sel_hscif0[0]	+ select pin HSCIF0_HRX for function HRX0 + select pin HSCIF0_HSCK for function HSCK0 + select pin HSCIF0_HTX for function HTX0	+ select pin A14 for function HRX0_B + select pin A15 for function HTX0_B + select pin A16 for function HSCK0_B			

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_hscif1[0]	+ select pin HSCIF1_HCTS_N for function HCTS1_N + select pin HSCIF1_HRTS_N for function HRTS1_N + select pin HSCIF1_HRX for function HRX1 + select pin HSCIF1_HTX for function HTX1	+ select pin SSI_SCK2 for function HTX1_B + select pin SSI_SDATA1 for function HRX1_B + select pin SSI_SDATA2 for function HRTS1_N_B + select pin SSI_WS2 for function HCTS1_N_B			

Legend: – Setting prohibited

5.3.25 Module Select Register 3 (MOD_SEL3)

Function: MOD_SEL3 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF and SSI is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. When ssi8 and ssi7 (in MOD_SEL3 register) are to be used simultaneously, the values of sel_ssi8[0] and sel_ssi7[0] must be the same so that the selected pins belong to the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_scif 0[1]	sel_scif 0[0]	sel_scif 1[1]	sel_scif 1[0]	sel_scif 2[1]	sel_scif 2[0]	sel_scif 3[0]	sel_scif 4[2]	sel_scif 4[1]	sel_scif 4[0]	sel_scif 5[1]	sel_scif 5[0]	sel_ssi 1[0]	sel_ssi 2[0]	sel_ssi 4[0]	sel_ssi 5[0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ssi 6[0]	sel_ssi 7[0]	sel_ssi 8[0]	sel_ssi 9[0]	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_scif0[1:0]	+ select pin EX_WAIT0 for function SCIF_CLK + select pin MMC_D6 for function SCIF0_RXD + select pin MMC_D7 for function SCIF0_TX0	+ select pin HSCIF0_HSCK for function SCIF_CLK_B + select pin VI0_HSYNC_N for function SCIF0_RXD_B + select pin VI0_VSYNC_N for function SCIF0_TXD_B	+ select pin I2C0_SCL for function SCIF0_RXD_C + select pin I2C0_SDA for function SCIF0_TXD_C	+ select pin HSCIF0_HCTS_N for function SCIF0_RXD_D + select pin HSCIF0_HRTS_N for function SCIF0_TXD_D	
sel_scif1[1:0]	+ select pin SCIF1_RXD for function SCIF1_RXD + select pin SCIF1_SCK for function SCIF1_SCK + select pin SCIF1_TXD for function SCIF1_TXD	+ select pin SSI_SCK1 for function SCIF1_RXD_B + select pin SSI_SDATA8 for function SCIF1_SCK_B + select pin SSI_WS1 for function SCIF1_TXD_B	+ select pin D10 for function SCIF1_SCK_C + select pin D11 for function SCIF1_RXD_C + select pin D12 for function SCIF1_TXD_C		
sel_scif2[2:0]	+ select pin SCIF2_RXD for function SCIF2_RXD + select pin SCIF2_SCK for function SCIF2_SCK + select pin SCIF2_TXD for function SCIF2_TXD	+ select pin SSI_SCK9 for function SCIF2_SCK_B + select pin SSI_SDATA9 for function SCIF2_TXD_B + select pin SSI_WS9 for function SCIF2_RXD_B	+ select pin ETH_REF_CLK for function SCIF2_SCK_C + select pin ETH_TXD1 for function SCIF2_RXD_C + select pin ETH_TX_EN for function SCIF2_TXD_C		
sel_scif3[0]	+ select pin SCIF3_RXD for function SCIF3_RXD + select pin SCIF3_SCK for function SCIF3_SCK + select pin SCIF3_TXD for function SCIF3_TXD	+ select pin ETH_MAGIC for function SCIF3_SCK_B + select pin ETH_MDC for function SCIF3_TXD_B + select pin ETH_TXD0 for function SCIF3_RXD_B			
sel_scif4[2:0]	+ select pin I2C1_SCL for function SCIF4_RXD + select pin I2C1_SDA for function SCIF4_TXD	+ select pin D5 for function SCIF4_RXD_B + select pin D6 for function SCIF4_TXD_B	+ select pin EX_CS2_N for function SCIF4_RXD_C + select pin EX_CS3_N for function SCIF4_TXD_C	+ select pin ETH_LINK for function SCIF4_TXD_D + select pin ETH_RXD1 for function SCIF4_RXD_D	+ select pin A17 for function SCIF4_RXD_E + select pin A18 for function SCIF4_TXD_E

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)
sel_scif5[1:0]	+ select pin MSIOF0_RXD for function SCIF5_RXD + select pin MSIOF0_TXD for function SCIF5_TXD	+ select pin D3 for function SCIF5_RXD_B + select pin D4 for function SCIF5_TXD_B	+ select pin DU0_DR0 for function SCIF5_RXD_C + select pin DU0_DR1 for function SCIF5_TXD_C	+ select pin SSI_SCK0129 for function SCIF5_RXD_D + select pin SSI_WS0129 for function SCIF5_TXD_D	
sel_ssi1[0]	+ select pin SSI_SCK1 for function SSI_SCK1 + select pin SSI_SDATA1 for function SSI_SDATA1 + select pin SSI_WS1 for function SSI_WS1	+ select pin HSCIF1_HCTS_N for function SSI_SCK1_B + select pin HSCIF1_HRTS_N for function SSI_WS1_B + select pin SCIF1_SCK for function SSI_SDATA1_B			
sel_ssi2[0]	+ select pin SSI_SCK2 for function SSI_SCK2 + select pin SSI_SDATA2 for function SSI_SDATA2 + select pin SSI_WS2 for function SSI_WS2	+ select pin SCIF1_RXD for function SSI_SCK2_B + select pin SCIF1_TXD for function SSI_WS2_B + select pin SCIF2_RXD for function SSI_SDATA2_B			
sel_ssi4[0]	+ select pin SSI_SCK4 for function SSI_SCK4 + select pin SSI_SDATA4 for function SSI_SDATA4 + select pin SSI_WS4 for function SSI_WS4	+ select pin I2C2_SCL for function SSI_SDATA4_B + select pin SCIF3_RXD for function SSI_SCK4_B + select pin SCIF3_TXD for function SSI_WS4_B			
sel_ssi5[0]	+ select pin SSI_SCK5 for function SSI_SCK5 + select pin SSI_SDATA5 for function SSI_SDATA5 + select pin SSI_WS5 for function SSI_WS5	+ select pin ETH_REF_CLK for function SSI_SCK5_B + select pin ETH_TXD1 for function SSI_WS5_B + select pin ETH_TX_EN for function SSI_SDATA5_B			
sel_ssi6[0]	+ select pin SSI_SCK6 for function SSI_SCK6 + select pin SSI_SDATA6 for function SSI_SDATA6 + select pin SSI_WS6 for function SSI_WS6	+ select pin ETH_MAGIC for function SSI_SCK6_B + select pin ETH_MDC for function SSI_SDATA6_B + select pin ETH_TXD0 for function SSI_WS6_B			
sel_ssi7[0]	+ select pin SSI_SCK78 for function SSI_SCK78 + select pin SSI_SDATA7 for function SSI_SDATA7 + select pin SSI_WS78 for function SSI_WS78	+ select pin HSCIF0_HCTS_N for function SSI_SDATA7_B + select pin HSCIF0_HRX for function SSI_SCK78_B + select pin HSCIF0_HTX for function SSI_WS78_B			
sel_ssi8[0]	+ select pin SSI_SDATA8 for function SSI_SDATA8	+ select pin HSCIF0_HRTS_N for function SSI_SDATA8_B			
sel_ssi9[0]	+ select pin SSI_SCK9 for function SSI_SCK9 + select pin SSI_SDATA9 for function SSI_SDATA9 + select pin SSI_WS9 for function SSI_WS9	+ select pin SCIF2_SCK for function SSI_WS9_B + select pin SCIF2_TXD for function SSI_SCK9_B + select pin SCIF3_SCK for function SSI_SDATA9_B			

Legend: - Setting prohibited

5.3.26 LSI Pin Pull-Up Control Register 0 (PUPR0)

Function: PUPR0 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR0 [31]	PUPR0 [30]	PUPR0 [29]	PUPR0 [28]	PUPR0 [27]	PUPR0 [26]	PUPR0 [25]	PUPR0 [24]	PUPR0 [23]	PUPR0 [22]	PUPR0 [21]	PUPR0 [20]	PUPR0 [19]	PUPR0 [18]	PUPR0 [17]	PUPR0 [16]
Initial value:	0	1	0	1	1	1	0	1	0	1	1	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR0 [15]	PUPR0 [14]	PUPR0 [13]	PUPR0 [12]	PUPR0 [11]	PUPR0 [10]	PUPR0 [9]	PUPR0 [8]	PUPR0 [7]	PUPR0 [6]	PUPR0 [5]	PUPR0 [4]	PUPR0 [3]	PUPR0 [2]	PUPR0 [1]	PUPR0 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR0[31:0]	H'5D60 FFFF	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up/down function is disabled. 1: Pull-up/down function is enabled.

Bit Name	Set Value = 1
PUPR0[31]	A15 is pull up
PUPR0[30]	A14 is pull up
PUPR0[29]	A13 is pull up
PUPR0[28]	A12 is pull up
PUPR0[27]	A11 is pull up
PUPR0[26]	A10 is pull up
PUPR0[25]	A9 is pull up
PUPR0[24]	A8 is pull up
PUPR0[23]	A7 is pull up
PUPR0[22]	A6 is pull up
PUPR0[21]	A5 is pull up
PUPR0[20]	A4 is pull up
PUPR0[19]	A3 is pull up
PUPR0[18]	A2 is pull up
PUPR0[17]	A1 is pull up
PUPR0[16]	A0 is pull up
PUPR0[15]	D15 is pull up
PUPR0[14]	D14 is pull up
PUPR0[13]	D13 is pull up
PUPR0[12]	D12 is pull up
PUPR0[11]	D11 is pull up
PUPR0[10]	D10 is pull up
PUPR0[9]	D9 is pull up
PUPR0[8]	D8 is pull up
PUPR0[7]	D7 is pull up

Bit Name	Set Value = 1
PUPR0[6]	D6 is pull up
PUPR0[5]	D5 is pull up
PUPR0[4]	D4 is pull up
PUPR0[3]	D3 is pull up
PUPR0[2]	D2 is pull up
PUPR0[1]	D1 is pull up
PUPR0[0]	D0 is pull up

5.3.27 LSI Pin Pull-Up Control Register 1 (PUPR1)

Function: PUPR1 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR1 [31]	PUPR1 [30]	PUPR1 [29]	PUPR1 [28]	PUPR1 [27]	PUPR1 [26]	PUPR1 [25]	PUPR1 [24]	PUPR1 [23]	PUPR1 [22]	PUPR1 [21]	PUPR1 [20]	PUPR1 [19]	PUPR1 [18]	PUPR1 [17]	PUPR1 [16]
Initial value:	0	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR1 [15]	PUPR1 [14]	PUPR1 [13]	PUPR1 [12]	PUPR1 [11]	PUPR1 [10]	PUPR1 [9]	PUPR1 [8]	PUPR1 [7]	PUPR1 [6]	PUPR1 [5]	PUPR1 [4]	PUPR1 [3]	PUPR1 [2]	PUPR1 [1]	PUPR1 [0]
Initial value:	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR1[31:0]	H'7FD8 3FF3	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up/down function is disabled. 1: Pull-up/down function is enabled.

Bit Name	Set Value = 1
PUPR1[31]	-
PUPR1[30]	ACK is pull down
PUPR1[29]	EX_CS5_N is pull up
PUPR1[28]	EX_CS3_N is pull up
PUPR1[27]	EX_CS1_N is pull up
PUPR1[26]	CS1_N_A26 is pull up
PUPR1[25]	TDI is pull up
PUPR1[24]	TMS is pull up
PUPR1[23]	TCK is pull up
PUPR1[22]	TRST_N is pull up
PUPR1[21]	DACK0 is pull up
PUPR1[20]	DREQ0_N is pull up
PUPR1[19]	EX_WAIT0 is pull up
PUPR1[18]	WE1_N is pull up
PUPR1[17]	WE0_N is pull up
PUPR1[16]	RD_WR_N is pull up
PUPR1[15]	RD_N is pull up
PUPR1[14]	BS_N is pull up
PUPR1[13]	EX_CS4_N is pull up
PUPR1[12]	EX_CS2_N is pull up
PUPR1[11]	EX_CS0_N is pull up
PUPR1[10]	CS0_N is pull up
PUPR1[9]	A25 is pull up
PUPR1[8]	A24 is pull up
PUPR1[7]	A23 is pull up

Bit Name	Set Value = 1
PUPR1[6]	A22 is pull up
PUPR1[5]	A21 is pull up
PUPR1[4]	A20 is pull up
PUPR1[3]	A19 is pull up
PUPR1[2]	A18 is pull up
PUPR1[1]	A17 is pull up
PUPR1[0]	A16 is pull up

5.3.28 LSI Pin Pull-Up Control Register 2 (PUPR2)

Function: PUPR2 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR2 [31]	PUPR2 [30]	PUPR2 [29]	PUPR2 [28]	PUPR2 [27]	PUPR2 [26]	PUPR2 [25]	PUPR2 [24]	PUPR2 [23]	PUPR2 [22]	PUPR2 [21]	PUPR2 [20]	PUPR2 [19]	PUPR2 [18]	PUPR2 [17]	PUPR2 [16]
Initial value:	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR2 [15]	PUPR2 [14]	PUPR2 [13]	PUPR2 [12]	PUPR2 [11]	PUPR2 [10]	PUPR2 [9]	PUPR2 [8]	PUPR2 [7]	PUPR2 [6]	PUPR2 [5]	PUPR2 [4]	PUPR2 [3]	PUPR2 [2]	PUPR2 [1]	PUPR2 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR2[31:0]	H'27FF FFFF	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up/down function is disabled. 1: Pull-up/down function is enabled.

Bit Name	Set Value = 1
PUPR2[31]	DU0_CDE is pull up
PUPR2[30]	DU0_DISP is pull up
PUPR2[29]	DU0_EXODDF_DU0_ODDF_DISP_CDE is pull up
PUPR2[28]	DU0_EXVSYNC_DU0_VSYNC is pull up
PUPR2[27]	DU0_EXHSYNC_DU0_HSYNC is pull up
PUPR2[26]	DU0_DOTCLKOUT1 is pull up
PUPR2[25]	DU0_DOTCLKOUT0 is pull up
PUPR2[24]	DU0_DOTCLKIN is pull up
PUPR2[23]	DU0_DB7 is pull up
PUPR2[22]	DU0_DB6 is pull up
PUPR2[21]	DU0_DB5 is pull up
PUPR2[20]	DU0_DB4 is pull up
PUPR2[19]	DU0_DB3 is pull up
PUPR2[18]	DU0_DB2 is pull up
PUPR2[17]	DU0_DB1 is pull up
PUPR2[16]	DU0_DB0 is pull up
PUPR2[15]	DU0_DG7 is pull up
PUPR2[14]	DU0_DG6 is pull up
PUPR2[13]	DU0_DG5 is pull up
PUPR2[12]	DU0_DG4 is pull up
PUPR2[11]	DU0_DG3 is pull up
PUPR2[10]	DU0_DG2 is pull up
PUPR2[9]	DU0_DG1 is pull up
PUPR2[8]	DU0_DG0 is pull up
PUPR2[7]	DU0_DR7 is pull up

Bit Name	Set Value = 1
PUPR2[6]	DU0_DR6 is pull up
PUPR2[5]	DU0_DR5 is pull up
PUPR2[4]	DU0_DR4 is pull up
PUPR2[3]	DU0_DR3 is pull up
PUPR2[2]	DU0_DR2 is pull up
PUPR2[1]	DU0_DR1 is pull up
PUPR2[0]	DU0_DR0 is pull up

5.3.29 LSI Pin Pull-Up Control Register 3 (PUPR3)

Function: PUPR3 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR3 [31]	PUPR3 [30]	PUPR3 [29]	PUPR3 [28]	PUPR3 [27]	PUPR3 [26]	PUPR3 [25]	PUPR3 [24]	PUPR3 [23]	PUPR3 [22]	PUPR3 [21]	PUPR3 [20]	PUPR3 [19]	PUPR3 [18]	PUPR3 [17]	PUPR3 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR3 [15]	PUPR3 [14]	PUPR3 [13]	PUPR3 [12]	PUPR3 [11]	PUPR3 [10]	PUPR3 [9]	PUPR3 [8]	PUPR3 [7]	PUPR3 [6]	PUPR3 [5]	PUPR3 [4]	PUPR3 [3]	PUPR3 [2]	PUPR3 [1]	PUPR3 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR3[31:0]	H'FFFF FFFF	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR3[31]	I2C1_SDA is pull up
PUPR3[30]	I2C1_SCL is pull up
PUPR3[29]	I2C0_SDA is pull up
PUPR3[28]	I2C0_SCL is pull up
PUPR3[27]	HSCIF0_HSCK is pull up
PUPR3[26]	HSCIF0_HRTS_N is pull up
PUPR3[25]	HSCIF0_HCTS_N is pull up
PUPR3[24]	HSCIF0_HTX is pull up
PUPR3[23]	HSCIF0_HRX is pull up
PUPR3[22]	ETH_MDC is pull up
PUPR3[21]	ETH_TXD0 is pull up
PUPR3[20]	ETH_MAGIC is pull up
PUPR3[19]	ETH_TX_EN is pull up
PUPR3[18]	ETH_TXD1 is pull up
PUPR3[17]	ETH_REF_CLK is pull up
PUPR3[16]	ETH_LINK is pull up
PUPR3[15]	ETH_RXD1 is pull up
PUPR3[14]	ETH_RXD0 is pull up
PUPR3[13]	ETH_RX_ER is pull up
PUPR3[12]	ETH_CRS_DV is pull up
PUPR3[11]	ETH_MDIO is pull up
PUPR3[10]	VI0_VSYNC_N is pull up
PUPR3[9]	VI0_HSYNC_N is pull up
PUPR3[8]	VI0_FIELD is pull up
PUPR3[7]	VI0_CLKENB is pull up

Bit Name	Set Value = 1
PUPR3[6]	VI0_DATA7_VI0_B7 is pull up
PUPR3[5]	VI0_DATA6_VI0_B6 is pull up
PUPR3[4]	VI0_DATA5_VI0_B5 is pull up
PUPR3[3]	VI0_DATA4_VI0_B4 is pull up
PUPR3[2]	VI0_DATA3_VI0_B3 is pull up
PUPR3[1]	VI0_DATA2_VI0_B2 is pull up
PUPR3[0]	VI0_DATA1_VI0_B1 is pull up

5.3.30 LSI Pin Pull-Up Control Register 4 (PUPR4)

Function: PUPR4 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR4 [31]	PUPR4 [30]	PUPR4 [29]	PUPR4 [28]	PUPR4 [27]	PUPR4 [26]	PUPR4 [25]	PUPR4 [24]	PUPR4 [23]	PUPR4 [22]	PUPR4 [21]	PUPR4 [20]	PUPR4 [19]	PUPR4 [18]	PUPR4 [17]	PUPR4 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR4 [15]	PUPR4 [14]	PUPR4 [13]	PUPR4 [12]	PUPR4 [11]	PUPR4 [10]	PUPR4 [9]	PUPR4 [8]	PUPR4 [7]	PUPR4 [6]	PUPR4 [5]	PUPR4 [4]	PUPR4 [3]	PUPR4 [2]	PUPR4 [1]	PUPR4 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR4[31:0]	H'FFFF FFFF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR4[31]	SSI_SCK0129 is pull up
PUPR4[30]	SSI_SDATA7 is pull up
PUPR4[29]	SSI_WS78 is pull up
PUPR4[28]	SSI_SCK78 is pull up
PUPR4[27]	SSI_SDATA6 is pull up
PUPR4[26]	SSI_WS6 is pull up
PUPR4[25]	SSI_SCK6 is pull up
PUPR4[24]	SSI_SDATA5 is pull up
PUPR4[23]	SSI_WS5 is pull up
PUPR4[22]	SSI_SCK5 is pull up
PUPR4[21]	I2C2_SDA is pull up
PUPR4[20]	I2C2_SCL is pull up
PUPR4[19]	SCIF3_TXD is pull up
PUPR4[18]	SCIF3_RXD is pull up
PUPR4[17]	SCIF3_SCK is pull up
PUPR4[16]	SCIF2_SCK is pull up
PUPR4[15]	SCIF2_TXD is pull up
PUPR4[14]	SCIF2_RXD is pull up
PUPR4[13]	SCIF1_TXD is pull up
PUPR4[12]	SCIF1_RXD is pull up
PUPR4[11]	SCIF1_SCK is pull up
PUPR4[10]	HSCIF1_HRTS_N is pull up
PUPR4[9]	HSCIF1_HCTS_N is pull up
PUPR4[8]	HSCIF1_HSCK is pull up
PUPR4[7]	HSCIF1_HTX is pull up

Bit Name	Set Value = 1
PUPR4[6]	HSCIF1_HRX is pull up
PUPR4[5]	MSIOF0_SS2 is pull up
PUPR4[4]	MSIOF0_SS1 is pull up
PUPR4[3]	MSIOF0_SYNC is pull up
PUPR4[2]	MSIOF0_SCK is pull up
PUPR4[1]	MSIOF0_TXD is pull up
PUPR4[0]	MSIOF0_RXD is pull up

5.3.31 LSI Pin Pull-Up Control Register 5 (PUPR5)

Function: PUPR5 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR5 [31]	PUPR5 [30]	PUPR5 [29]	PUPR5 [28]	PUPR5 [27]	PUPR5 [26]	PUPR5 [25]	PUPR5 [24]	PUPR5 [23]	PUPR5 [22]	PUPR5 [21]	PUPR5 [20]	PUPR5 [19]	PUPR5 [18]	PUPR5 [17]	PUPR5 [16]
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR5 [15]	PUPR5 [14]	PUPR5 [13]	PUPR5 [12]	PUPR5 [11]	PUPR5 [10]	PUPR5 [9]	PUPR5 [8]	PUPR5 [7]	PUPR5 [6]	PUPR5 [5]	PUPR5 [4]	PUPR5 [3]	PUPR5 [2]	PUPR5 [1]	PUPR5 [0]
Initial value:	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR5[31:0]	H'00FF FF1F	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR5[31]	-
PUPR5[30]	-
PUPR5[29]	-
PUPR5[28]	-
PUPR5[27]	-
PUPR5[26]	-
PUPR5[25]	-
PUPR5[24]	-
PUPR5[23]	VI0_DATA0_VI0_B0 is pull up
PUPR5[22]	VI0_CLK is pull up
PUPR5[21]	AUDIO_CLKOUT is pull up
PUPR5[20]	AUDIO_CLKC is pull up
PUPR5[19]	AUDIO_CLKB is pull up
PUPR5[18]	AUDIO_CLKA is pull up
PUPR5[17]	SSI_SDATA9 is pull up
PUPR5[16]	SSI_WS9 is pull up
PUPR5[15]	SSI_SCK9 is pull up
PUPR5[14]	SSI_SDATA2 is pull up
PUPR5[13]	SSI_WS2 is pull up
PUPR5[12]	SSI_SCK2 is pull up
PUPR5[11]	SSI_SDATA1 is pull up
PUPR5[10]	SSI_WS1 is pull up
PUPR5[9]	SSI_SCK1 is pull up
PUPR5[8]	SSI_SDATA8 is pull up
PUPR5[7]	-

Bit Name	Set Value = 1
PUPR5[6]	-
PUPR5[5]	-
PUPR5[4]	SSI_SDATA3 is pull up
PUPR5[3]	SSI_WS34 is pull up
PUPR5[2]	SSI_SCK34 is pull up
PUPR5[1]	SSI_SDATA0 is pull up
PUPR5[0]	SSI_WS0129 is pull up

5.3.32 LSI Pin Pull-Up Control Register 6 (PUPR6)

Function: PUPR6 performs on/off control of the pull-up resistors.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR6 [31]	PUPR6 [30]	PUPR6 [29]	PUPR6 [28]	PUPR6 [27]	PUPR6 [26]	PUPR6 [25]	PUPR6 [24]	PUPR6 [23]	PUPR6 [22]	PUPR6 [21]	PUPR6 [20]	PUPR6 [19]	PUPR6 [18]	PUPR6 [17]	PUPR6 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR6 [15]	PUPR6 [14]	PUPR6 [13]	PUPR6 [12]	PUPR6 [11]	PUPR6 [10]	PUPR6 [9]	PUPR6 [8]	PUPR6 [7]	PUPR6 [6]	PUPR6 [5]	PUPR6 [4]	PUPR6 [3]	PUPR6 [2]	PUPR6 [1]	PUPR6 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR6[31:0]	H'0000 0000	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR6[31]	-
PUPR6[30]	-
PUPR6[29]	-
PUPR6[28]	-
PUPR6[27]	-
PUPR6[26]	-
PUPR6[25]	-
PUPR6[24]	-
PUPR6[23]	MMC_D7 is pull up
PUPR6[22]	MMC_D6 is pull up
PUPR6[21]	MMC_D5 is pull up
PUPR6[20]	MMC_D4 is pull up
PUPR6[19]	MMC_D3 is pull up
PUPR6[18]	MMC_D2 is pull up
PUPR6[17]	MMC_D1 is pull up
PUPR6[16]	MMC_D0 is pull up
PUPR6[15]	MMC_CMD is pull up
PUPR6[14]	-
PUPR6[13]	SD1_WP is pull up
PUPR6[12]	SD1_CD is pull up
PUPR6[11]	SD1_DATA3 is pull up
PUPR6[10]	SD1_DATA2 is pull up
PUPR6[9]	SD1_DATA1 is pull up
PUPR6[8]	SD1_DATA0 is pull up
PUPR6[7]	SD1_CMD is pull up

Bit Name	Set Value = 1
PUPR6[6]	SD0_WP is pull up
PUPR6[5]	SD0_CD is pull up
PUPR6[4]	SD0_DATA3 is pull up
PUPR6[3]	SD0_DATA2 is pull up
PUPR6[2]	SD0_DATA1 is pull up
PUPR6[1]	SD0_DATA0 is pull up
PUPR6[0]	SD0_CMD is pull up

5.3.33 SD Control Register 0 (IOCTRL0)

Function: IOCTRL0 controls the driving abilities of pins in use for the MMC and SD0 interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	drv2_mmcclk	drv1_mmcclk	drv2_mmccmd	drv1_mmccmd	drv2_mmcd0	drv1_mmcd0	drv2_mmcd1	drv1_mmcd1	drv2_mmcd2	drv1_mmcd2	drv2_mmcd3	drv1_mmcd3	drv2_mmcd4	drv1_mmcd4	drv2_mmcd5	drv1_mmcd5
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	drv2_mmcd6	drv1_mmcd6	drv2_mmcd7	drv1_mmcd7	drv2_sd0cd	drv1_sd0cd	drv2_sd0clk	drv1_sd0clk	drv2_sd0cmd	drv1_sd0cmd	drv2_sd0data0	drv1_sd0data0	drv2_sd0data1	drv1_sd0data1	drv2_sd0data2	drv1_sd0data2
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	drv2_mmcclk	1	R/W	MMC_CLK Setting.
30	drv1_mmcclk	1	R/W	The value of these bits must be 11.
29	drv2_mmccmd	1	R/W	MMC_CMD Setting.
28	drv1_mmccmd	1	R/W	The value of these bits must be 11.
27	drv2_mmcd0	1	R/W	MMC_CD0 Setting.
26	drv1_mmcd0	1	R/W	The value of these bits must be 11.
25	drv2_mmcd1	1	R/W	MMC_CD1 Setting.
24	drv1_mmcd1	1	R/W	The value of these bits must be 11.
23	drv2_mmcd2	1	R/W	MMC_CD2 Setting.
22	drv1_mmcd2	1	R/W	The value of these bits must be 11.
21	drv2_mmcd3	1	R/W	MMC_CD3 Setting.
20	drv1_mmcd3	1	R/W	The value of these bits must be 11.
19	drv2_mmcd4	1	R/W	MMC_CD4 Setting.
18	drv1_mmcd4	1	R/W	The value of these bits must be 11.
17	drv2_mmcd5	1	R/W	MMC_CD5 Setting.
16	drv1_mmcd5	1	R/W	The value of these bits must be 11.
15	drv2_mmcd6	1	R/W	MMC_CD6 Setting.
14	drv1_mmcd6	1	R/W	The value of these bits must be 11.
13	drv2_mmcd7	1	R/W	MMC_CD7 Setting.
12	drv1_mmcd7	1	R/W	The value of these bits must be 11.
11	drv2_sd0cd	1	R/W	SD0_CD Setting.
10	drv1_sd0cd	1	R/W	The value of these bits must be 11.
9	drv2_sd0clk	1	R/W	SD0_CLK Setting.
8	drv1_sd0clk	1	R/W	The value of these bits must be 11.
7	drv2_sd0cmd	1	R/W	SD0_CMD Setting.
6	drv1_sd0cmd	1	R/W	The value of these bits must be 11.
5	drv2_sd0data0	1	R/W	SD0_DATA0 Setting.
4	drv1_sd0data0	1	R/W	The value of these bits must be 11.
3	drv2_sd0data1	1	R/W	SD0_DATA1 Setting.
2	drv1_sd0data1	1	R/W	The value of these bits must be 11.

Bit	Bit Name	Initial Value	R/W	Description
1	drv2_sd0data2	1	R/W	SD0_DATA2 Setting.
0	drv1_sd0data2	1	R/W	The value of these bits must be 11.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.34 SD Control Register 1 (IOCTRL1)

Function: IOCTRL1 controls the driving abilities of pins in use for the SD0 and SD1 interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	drv2_sd0data3	drv1_sd0data3	drv2_sd0wp	drv1_sd0wp	drv2_sd1cd	drv1_sd1cd	drv2_sd1clk	drv1_sd1clk	drv2_sd1cmd	drv1_sd1cmd	drv2_sd1data0	drv1_sd1data0	drv2_sd1data1	drv1_sd1data1	drv2_sd1data2	drv1_sd1data2
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	drv2_sd1data3	drv1_sd1data3	drv2_sd1wp	drv1_sd1wp	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	drv2_sd0data3	1	R/W	SD0_DATA3 Setting.
30	drv1_sd0data3	1	R/W	The value of these bits must be 11.
29	drv2_sd0wp	1	R/W	SD0_WP Setting.
28	drv1_sd0wp	1	R/W	The value of these bits must be 11.
27	drv2_sd1cd	1	R/W	SD1_CD Setting.
26	drv1_sd1cd	1	R/W	The value of these bits must be 11.
25	drv2_sd1clk	1	R/W	SD1_CLK Setting.
24	drv1_sd1clk	1	R/W	The value of these bits must be 11.
23	drv2_sd1cmd	1	R/W	SD1_CMD Setting.
22	drv1_sd1cmd	1	R/W	The value of these bits must be 11.
21	drv2_sd1data0	1	R/W	SD1_DATA0 Setting.
20	drv1_sd1data0	1	R/W	The value of these bits must be 11.
19	drv2_sd1data1	1	R/W	SD1_DATA1 Setting.
18	drv1_sd1data1	1	R/W	The value of these bits must be 11.
17	drv2_sd1data2	1	R/W	SD1_DATA2 Setting.
16	drv1_sd1data2	1	R/W	The value of these bits must be 11.
15	drv2_sd1data3	1	R/W	SD1_DATA3 Setting.
14	drv1_sd1data3	1	R/W	The value of these bits must be 11.
13	drv2_sd1wp	1	R/W	SD1_WP Setting.
12	drv1_sd1wp	1	R/W	The value of these bits must be 11.
11 to 0	—	—	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.35 TDSEL Control Register (IOCTRL2)

Function: IOCTRL2 controls the delay of clock of pins in use for the IRQ, DU and Ethernet interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	tdsel1_a10	tdsel0_a10	tdsel1_a16	tdsel0_a16	tdsel1_audioclkb	tdsel0_audioclkb	tdsel1_ethrxer	tdsel0_ethrxer	tdsel1_excs3n	tdsel0_excs3n	tdsel1_i2c1sda	tdsel0_i2c1sda	tdsel1_mmcclk	tdsel0_mmcclk	tdsel1_msiof0sck	tdsel0_msiof0sck
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	tdsel1_msiof0sync	tdsel0_msiof0sync	tdsel1_sd0clk	tdsel0_sd0clk	tdsel1_sd1clk	tdsel0_sd1clk	tdsel1_ssisdata0	tdsel0_ssisdata0	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	tdsel1_a10	0	R/W	A10 Setting.
30	tdsel0_a10	0	R/W	The value of these bits must be 00.
29	tdsel1_a16	0	R/W	A16 Setting.
28	tdsel0_a16	0	R/W	The value of these bits must be 00.
27	tdsel1_audioclkb	0	R/W	AUDIO_CLKB Setting.
26	tdsel0_audioclkb	0	R/W	The value of these bits must be 00.
25	tdsel1_ethrxer	0	R/W	ETH_RX_ER Setting.
24	tdsel0_ethrxer	0	R/W	The value of these bits must be 00.
23	tdsel1_excs3n	0	R/W	EX_CS3_N Setting.
22	tdsel0_excs3n	0	R/W	The value of these bits must be 00.
21	tdsel1_i2c1sda	0	R/W	I2C1_SDA Setting.
20	tdsel0_i2c1sda	0	R/W	The value of these bits must be 00.
19	tdsel1_mmcclk	0	R/W	MMC_CLK Setting.
18	tdsel0_mmcclk	0	R/W	The value of these bits must be 00.
17	tdsel1_msiof0sck	0	R/W	MSIOF0_SCK Setting.
16	tdsel0_msiof0sck	0	R/W	The value of these bits must be 00.
15	tdsel1_msiof0sync	0	R/W	MSIOF0_SYNC Setting.
14	tdsel0_msiof0sync	0	R/W	The value of these bits must be 00.
13	tdsel1_sd0clk	0	R/W	SD0_CLK Setting.
12	tdsel0_sd0clk	0	R/W	The value of these bits must be 00.
11	tdsel1_sd1clk	0	R/W	SD1_CLK Setting.
10	tdsel0_sd1clk	0	R/W	The value of these bits must be 00.
9	tdsel1_ssisdata0	0	R/W	SSI_SDATA0 Setting.
8	tdsel0_ssisdata0	0	R/W	The value of these bits must be 00.
7 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.36 POC Control Register (IOCTRL3)

Function: IOCTRL3 controls the IO voltage of pins in use for the SD interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	poc_mmcclk	poc_mmccmd	poc_mmcd0	poc_mmcd1	poc_mmcd2	poc_mmcd3	poc_mmcd4	poc_mmcd5	poc_sd0cd	poc_sd0clk	poc_sd0cmd	poc_sd0data0	poc_sd0data1	poc_sd0data2	poc_sd0data3	poc_sd0wp
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	poc_sd1cd	poc_sd1clk	poc_sd1cmd	poc_sd1data0	poc_sd1data1	poc_sd1data2	poc_sd1data3	poc_sd1wp	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

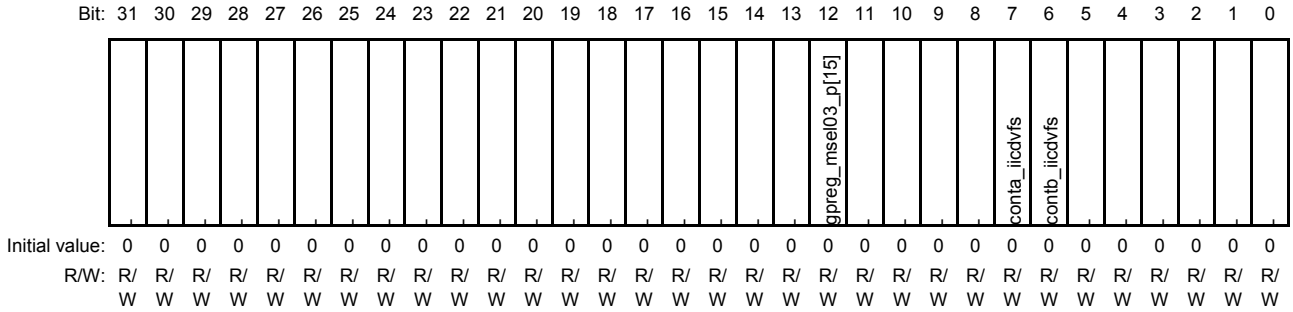
Bit	Bit Name	Initial Value	R/W	Description
31	poc_mmcclk (sd2clk)	1	R/W	Selecting IO voltage for the SD2 H'00: 1.8 V (VCCQ_MMC_SD2 = 1.8 V) H'FF: 3.3 V (VCCQ_MMC_SD2 = 3.3 V) Other than above: Setting prohibited Note: H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI that can be used either 3.3 V or 1.8 V. Note that the MMC IO can only be used with 3.3 V.
30	poc_mmccmd (sd2cmd)	1	R/W	
29	poc_mmcd0 (sd2data0)	1	R/W	
28	poc_mmcd1 (sd2data1)	1	R/W	
27	poc_mmcd2 (sd2data2)	1	R/W	
26	poc_mmcd3 (sd2data3)	1	R/W	
25	poc_mmcd4 (sd2cd)	1	R/W	
24	poc_mmcd5 (sd2wp)	1	R/W	
23	poc_sd0cd	1	R/W	Selecting IO voltage for the SD0 H'00: 1.8 V (VCCQ_SD0 = 1.8 V) H'FF: 3.3 V (VCCQ_SD0 = 3.3 V) Other than above: Setting prohibited Note: H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI that can be used either 3.3 V or 1.8 V.
22	poc_sd0clk	1	R/W	
21	poc_sd0cmd	1	R/W	
20	poc_sd0data0	1	R/W	
19	poc_sd0data1	1	R/W	
18	poc_sd0data2	1	R/W	
17	poc_sd0data3	1	R/W	
16	poc_sd0wp	1	R/W	
15	poc_sd1cd	1	R/W	Selecting IO voltage for the SD1 H'00: 1.8 V (VCCQ_SD1 = 1.8 V) H'FF: 3.3 V (VCCQ_SD1 = 3.3 V) Other than above: Setting prohibited Note: H'00 can only be set for the SDHI SDR50/SDR104 mode and the GPIO multiplexed with the SDHI that can be used either 3.3 V or 1.8V.
14	poc_sd1clk	1	R/W	
13	poc_sd1cmd	1	R/W	
12	poc_sd1data0	1	R/W	
11	poc_sd1data1	1	R/W	
10	poc_sd1data2	1	R/W	
9	poc_sd1data3	1	R/W	
8	poc_sd1wp	1	R/W	

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	—	All 0	R/W	—

Notes:
1. Any pin belongs to the same SD channel must be set to the same IO voltage as VCCQ_(MMC)_SDn. Even though setting different voltage for each pin of the same SD channel, it is impossible to change each pin voltage from the power supply voltage of the VCCQ_(MMC)_SDn.
2. When the VCCQ_(MMC)_SDn power supply voltage is 1.8-V to use the SDHI interface as SDR50/SDR104 mode or the GPIO (multiplexed with SDHI channel n pin) as 1.8-V IO, specify 1.8-V for IOCTRL6, then IO voltage of the SDHI channel n pins and multiplexed other function pins is all 1.8-V. In this condition, never input 3.3-V signal to these pins; if input 3.3-V signal, the LSI may be permanently damaged even though specifying the pin voltage to 3.3-V individually, furthermore, pull-up voltage of the unused pin which belongs to the same SD channel must be 1.8-V.
3. When the VCCQ_(MMC)_SDn power supply voltage is 3.3-V, to use the SDHI inter face as default mode, high-speed mode or other module function, specify 3.3-V for IOCTRL3, then IO voltage of the SDHI channel n and multiplexed other function pins is all 3.3-V. In this condition, output level of the pin is 3.3-V and if the external device can only operate with1.8-V, the external device may be permanently damaged even though specifying the pin voltage to 1.8-V individually.
4. For details of SDn related pin function settings, refer to following section.
   Section 5.3.8 GPSR 6, 5.3.9 IPSR 0 and 5.3.24 MOD_SEL2 (MMC_D[7:6]).
5. Some of the following module pins are multiplexed with the SDn pins.
   - INTC, CAN0, CAN1, MMC, SCIF0, I2C2
   They cannot be used with 1.8-V power supply (VCCQ_(MMC)_SDn) except for the multiplexed GPIO. Use them with 3.3-V power supply and set the corresponding VCCQ_(MMC)_SDn supply voltage to 3.3-V by IOCTRL3.
   For details of multiplexed pins of MMC/SDn, refer to Table 4.1, List of Multiplexed Pin Functions in section 4, Pin Multiplexing.
6. To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.37 IICDVFS and TDBG IO cell control register (IOCTRL7)

Function: IOCTRL7 controls the driving abilities of pins in use for the IIC and IICDVFS interfaces. This register is internal use and reserved; the value of this register should not be changed.



Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R/W	—
12	gpreg_msel03_p [15]	0	R/W	Debug monitor function: 0: Use DU pins for debug monitor function. 1: Use SDHI pins for debug monitor function.
11 to 8	—	All 0	R/W	—
7	conta_iicdvfs	0	R/W	Control TOF value of IICDVFS IO cell (TOF: Output fall time from VIH min to VIL max OR from 0.7VPU to 0.3VPU) 0: 0.3VPU 1: 0.7VPU
6	contb_iicdvfs	0	R/W	Control VIH/VIL value of IICDVFS IO cell (VIH: High level input voltage ; VIL: Low level input voltage) 0: VIL 1: VIH
5 to 0	—	All 0	R/W	—

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.4 Operation

5.4.1 Function Setting for Multiplexed Pins

Setting the LSI multiplexed pin setting mask register (PMMR) is necessary before setting each of the GPIO/peripheral function select registers 0 to 6 (GPSR0 to GPSR6) and peripheral function select registers 0 to 13 (IPSR0 to IPSR13). Specifically, the inverse of the value to be set in the select register must be written to the LSI multiplexed pin setting mask register. Otherwise, the GPIO/peripheral function select registers 0 to 6 (GPSR0 to GPSR6) and peripheral function select registers 0 to 13 (IPSR0 to IPSR13) cannot be set. IPSR0 to IPSR13, MOD_SEL, MOD_SEL2 and MOD_SEL3 registers shall be set before setting GPSR0 to GPSR6 registers in case that they need to be configured. MOD_SEL, MOD_SEL2 and MOD_SEL3 registers can be set either earlier or later than setting IPSR0 to IPSR13 registers.

(1) Procedure for changing pin function from GPIO to peripheral function

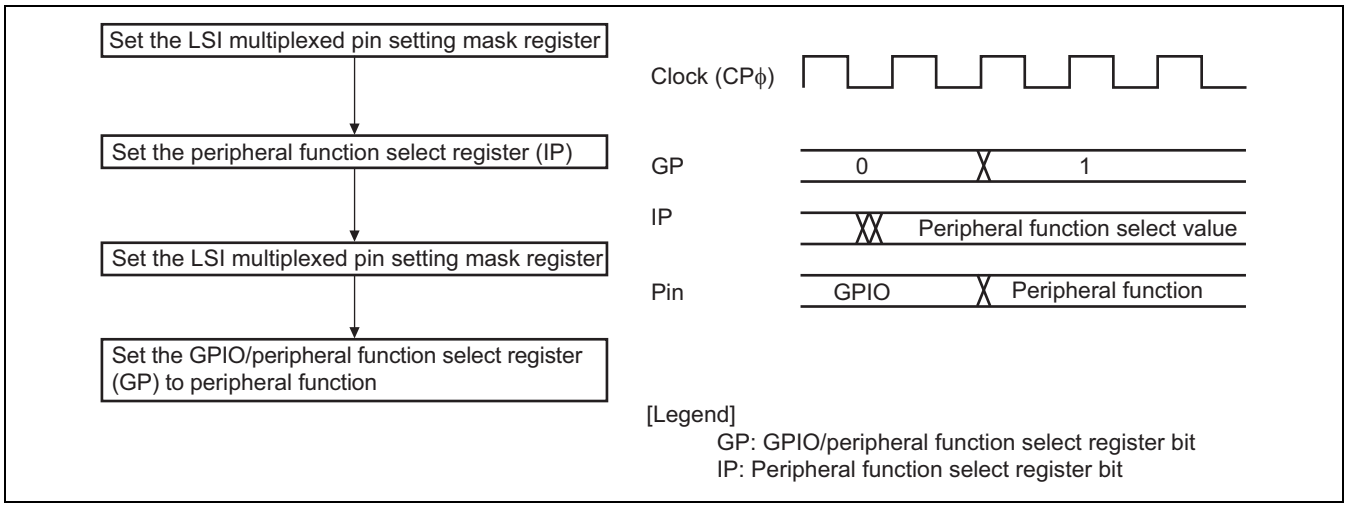


Figure 5.1 Procedure for Changing Pin Function from GPIO to Peripheral Function

(2) Procedure for changing pin function from peripheral function to GPIO

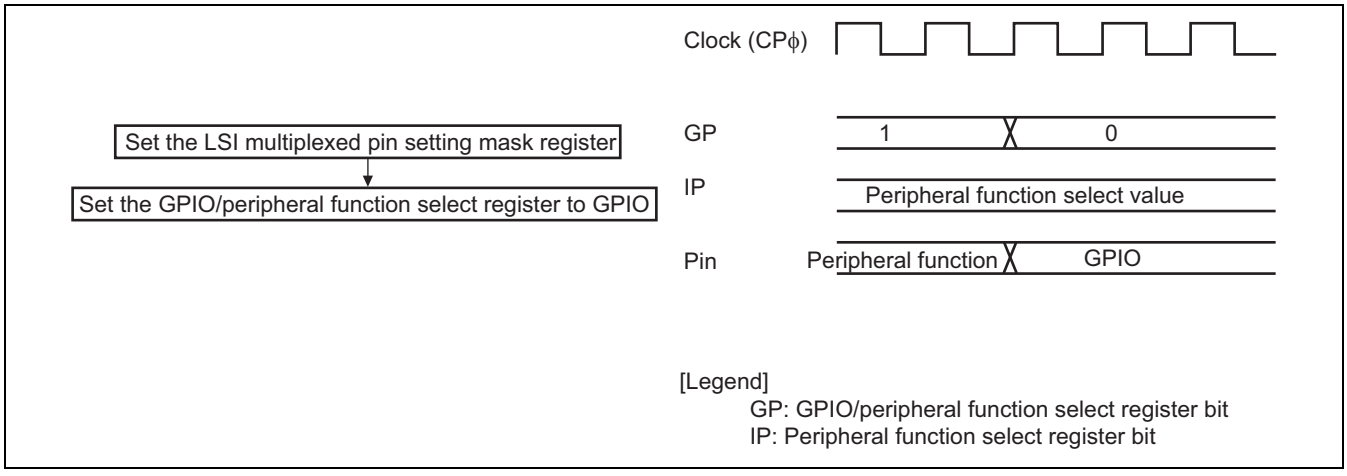


Figure 5.2 Procedure for Changing Pin Function from Peripheral function to GPIO

(3) Procedure 1 for changing pin function from one peripheral function to another peripheral function

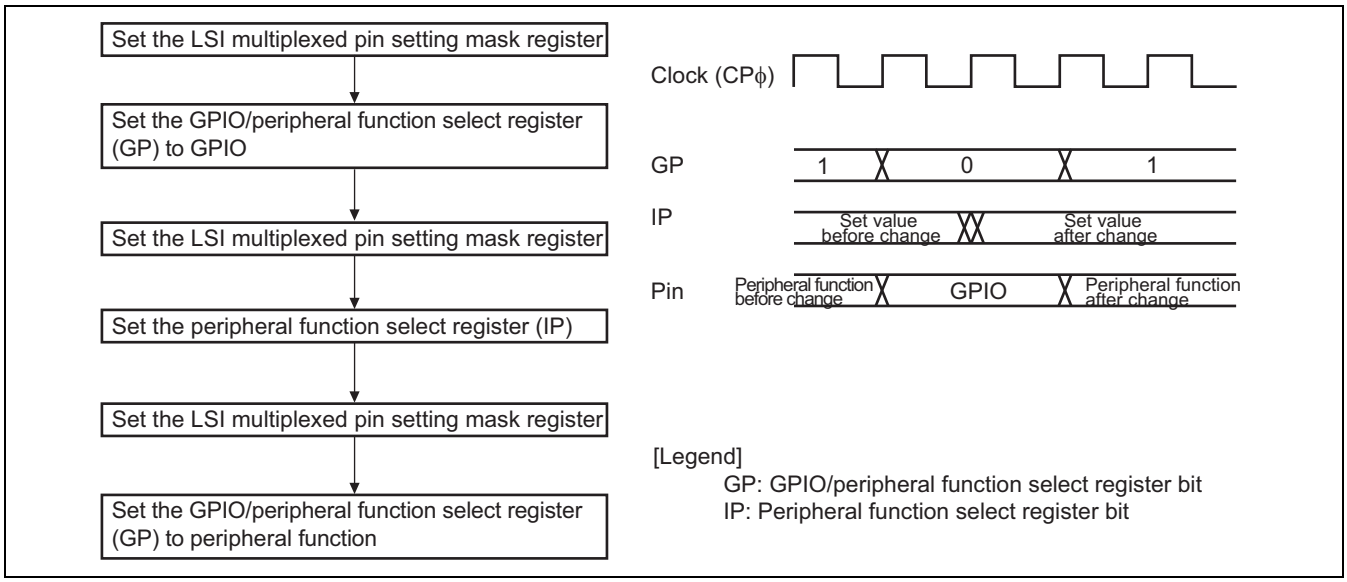


Figure 5.3 Procedure for Changing Pin Function from One Peripheral Function to Another Peripheral Function (with GPIO Setting)

5.4.2 Setting Pull-Up/Down Resistors

The LSI pin pull-up control registers 0 to 6 (PUPR0 to PUPR6) are used to switch the pull-up/down resistors on and off.

Main Revisions and Additions in this Edition

Minor revisions such as corrections of errors in spelling and modifications of wording are not included in the revision history.

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