

# 74ACT16646

## 16-Bit Transceiver/Register with 3-STATE Outputs

### General Description

The ACT16646 contains sixteen non-inverting bidirectional registered bus transceivers providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Each byte has separate control inputs which can be shorted together for full 16-bit operation. The DIR inputs determine the direction of data flow through the device. The CPAB and CPBA inputs load data into the registers on the LOW-to-HIGH transition.

### Features

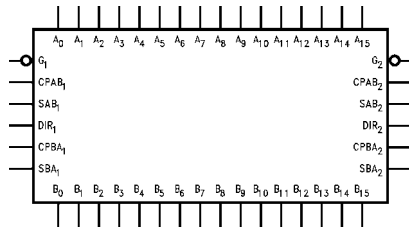
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- Separate control logic for each byte
- 16-bit version of the ACT646
- Outputs source/sink 24 mA
- TTL-compatible inputs

### Ordering Code:

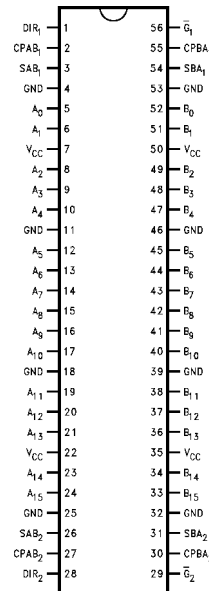
Order Number	Package Number	Package Description
74ACT16646SSC	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16646MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



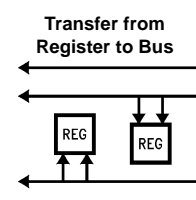
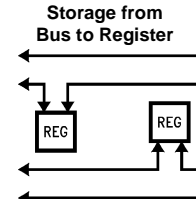
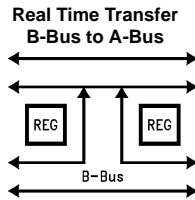
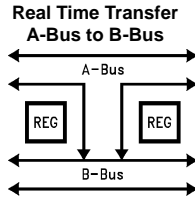
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Function Table

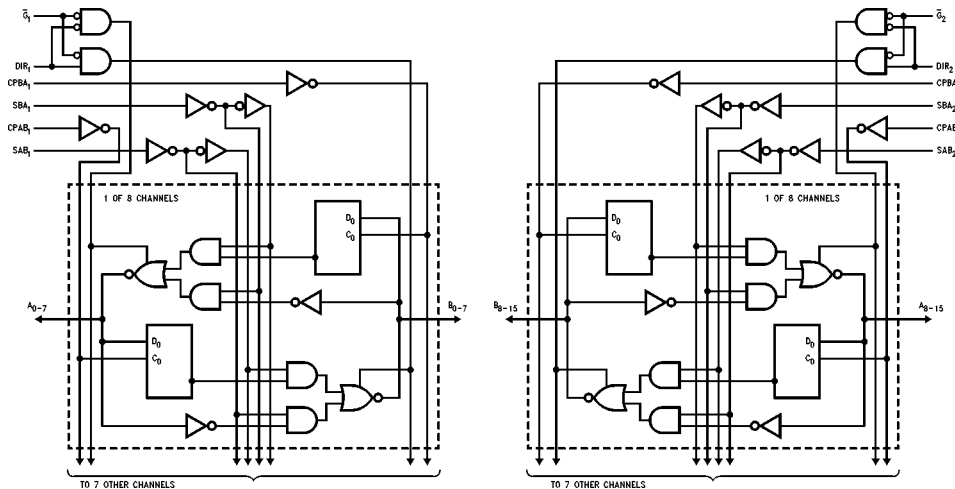
Inputs						Data I/O (Note 1)		Output Operation Mode
G <sub>1</sub>	DIR <sub>1</sub>	CPAB <sub>1</sub>	CPBA <sub>1</sub>	SAB <sub>1</sub>	SBA <sub>1</sub>	A <sub>0-7</sub>	B <sub>0-7</sub>	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↗	X	X	X			Clock A <sub>n</sub> Data into A Register
H	X	X	↗	X	X	Input	Output	Clock B <sub>n</sub> Data Into B Register
L	H	X	X	L	X			A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H	↗	X	L	X			Clock A <sub>n</sub> Data to A Register
L	H	H or L	X	H	X			A Register to B <sub>n</sub> (Stored Mode)
L	H	↗	X	H	X	Output	Input	Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	X	X	X	L			B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X	↗	X	L			Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	X	H			B Register to A <sub>n</sub> (Stored Mode)
L	L	X	↗	X	H			Clock B <sub>n</sub> into B Register and Output to A <sub>n</sub>

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level ↗ = LOW-to-HIGH Transition.

**Note 1:** The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs. Also applies to data I/O (A and B: 8-15) and #2 control pins.



Logic Diagram



**Absolute Maximum Ratings**(Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin	$\pm 50$ mA
Storage Temperature	-65°C to +150°C

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	125 mV/ns
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	

**Note 2:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
	5.5	1.5	2.0	2.0				
$V_{IL}$	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
	5.5	1.5	0.8	0.8				
$V_{OH}$	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$	
5.5		4.86	4.76	V	$I_{OH} = -24 \text{ mA}$ (Note 3)			
$V_{OL}$	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44	V	$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ (Note 3)	
5.5		0.36	0.44	V				
$I_{OZT}$	Maximum I/O Leakage Current	5.5		$\pm 0.5$	$\pm 5.0$	$\mu A$	$V_{IN} = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$	
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\mu A$	$V_I = V_{CC}, \text{GND}$	
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$	
$I_{CC}$	Max Quiescent Supply Current	5.5		8.0	80.0	$\mu A$	$V_{IN} = V_{CC}$ or GND	
$I_{OLD}$	Minimum Dynamic Output Current (Note 4)	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
$I_{OHD}$					-75	mA	$V_{OHD} = 3.85V \text{ Min}$	

**Note 3:** All outputs loaded; thresholds associated with output under test.

**Note 4:** Maximum test duration 2.0 ms; one output loaded at a time.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V) (Note 5)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		Units
			Min	Typ	Max	Min	Max	
t <sub>PHL</sub>	Propagation Delay	5.0	4.6	6.9	9.4	3.6	10.1	ns
t <sub>PLH</sub>	Clock to Bus		4.3	6.5	8.9	3.3	9.7	
t <sub>PHL</sub>	Propagation Delay	5.0	4.0	6.2	8.5	2.9	9.2	ns
t <sub>PLH</sub>	Bus to Bus		4.1	6.4	8.6	3.2	9.3	
t <sub>PHL</sub>	Propagation Delay	5.0	4.0	6.4	8.9	3.1	9.6	ns
t <sub>PLH</sub>	Select to Bus (w/An or Bn HIGH or LOW)		4.2	6.7	9.5	3.2	10.4	
t <sub>PZL</sub>	Enable Time	5.0	5.3	7.8	10.5	3.8	11.4	ns
t <sub>PZH</sub>	G to An/Bn		4.6	6.9	9.4	3.3	10.2	
t <sub>PLZ</sub>	Disable Time	5.0	3.0	5.5	8.1	2.3	8.6	ns
t <sub>PHZ</sub>	G to An/Bn		3.4	5.7	8.3	2.6	8.6	
t <sub>PZL</sub>	Enable Time	5.0	5.1	8.2	11.8	4.3	12.7	ns
t <sub>PZH</sub>	DIR to An/Bn		4.6	7.5	10.8	3.7	11.7	
t <sub>PLZ</sub>	Disable Time	5.0	2.9	5.8	9.2	2.0	9.8	ns
t <sub>PHZ</sub>	DIR to An/Bn		3.4	6.1	9.2	2.5	9.7	

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V.

## AC Operating Requirements

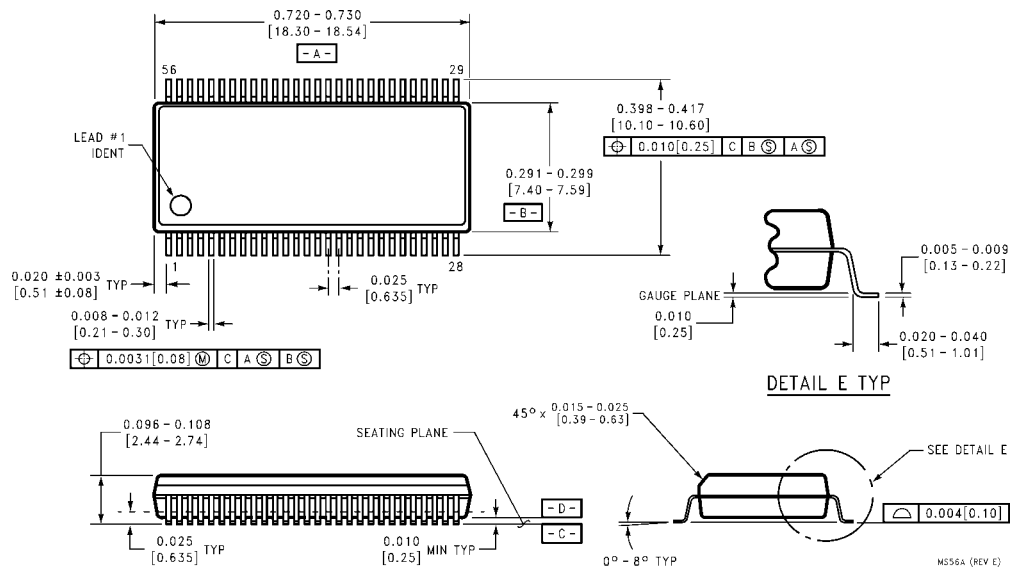
Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	Units
			Guaranteed Minimum		
t <sub>S</sub>	Setup Time, H or L Bus to Clock	5.0	3.0	3.0	ns
t <sub>H</sub>	Hold Time, H or L Bus to Clock	5.0	1.5	1.5	ns
t <sub>W</sub>	Clock Pulse Width H or L	5.0	4.0	4.0	ns

Note 6: Voltage Range 5.0 is 5.0V ± 0.5V.

## Capacitance

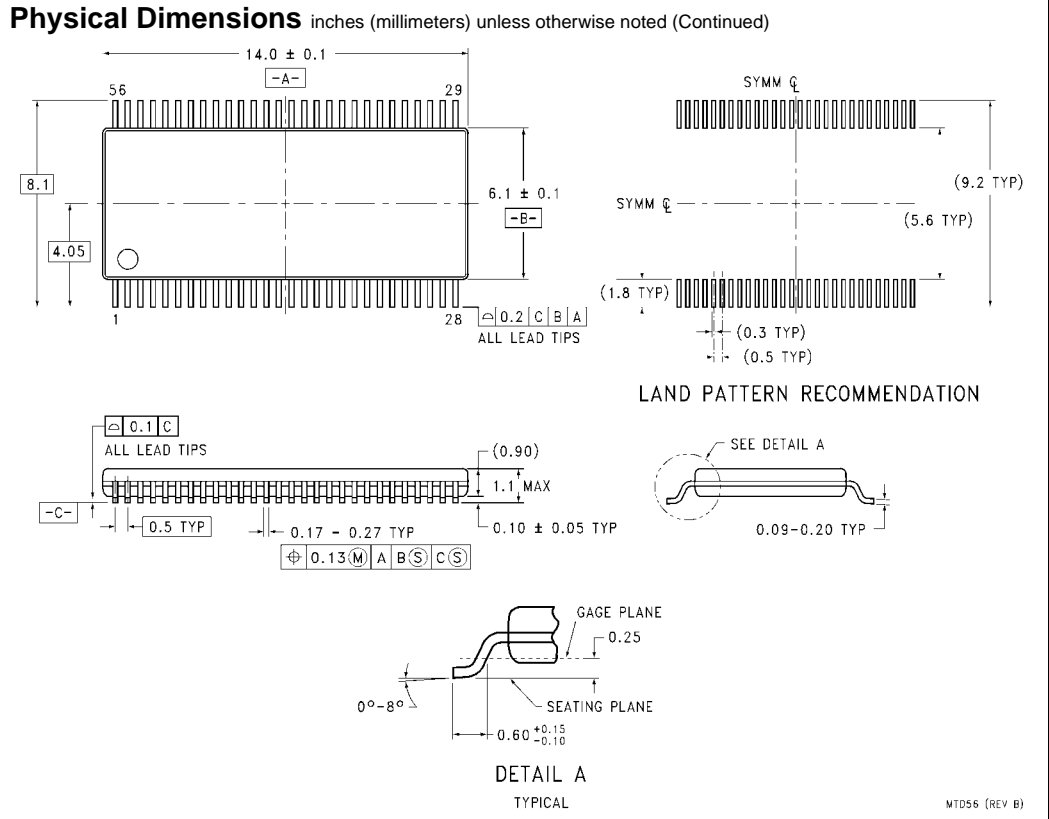
Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance	95	pF	V <sub>CC</sub> = 5.0V

**Physical Dimensions** inches (millimeters) unless otherwise noted



**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS56A**

MS56A (REV E)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD56

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