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August 2014

FDM3622
N-Channel PowerTrench® MOSFET
100V, 4.4A, 60mΩ

Features

- Max $r_{DS(on)}$ = 60mΩ at V_{GS} = 10V, I_D = 4.4A
- Max $r_{DS(on)}$ = 80mΩ at V_{GS} = 6.0V, I_D = 3.8A
- Low Miller Charge
- Low QRR Body Diode
- Optimized efficiency at high frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- Distributed Power Architectures and VRMs.
- Primary Switch for 24V and 48V Systems
- High Voltage Synchronous Rectifier
- Formerly developmental type 82744

Top

Bottom

Pin 1

MLP 3.3x3.3

S	1		8	D
S	2		7	D
S	3		6	D
G	4		5	D
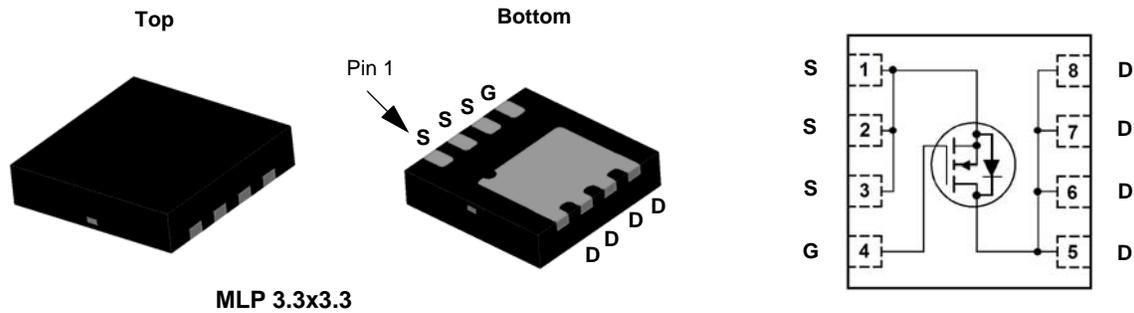
MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		100	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current -Continuous	(Note 1a)	4.4	A
	-Pulsed		20	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	54	mJ
P_D	Power Dissipation	(Note 1a)	2.1	W
	Power Dissipation	(Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDM3622	FDM3622	MLP 3.3x3.3	13"	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV$_{DSS}$	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	100			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V			1	μA
		T_J = 100°C			250	
I$_{GSS}$	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
V$_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2		4	V
r$_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 4.4A		44	60	mΩ
		V_{GS} = 6.0V, I_D = 3.8A		56	80	
		V_{GS} = 10V, I_D = 4.4A , T_J = 150°C		92	120	
Dynamic Characteristics						
C$_{iss}$	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		820	1090	pF
C$_{oss}$	Output Capacitance			125	170	pF
C$_{rss}$	Reverse Transfer Capacitance			35	55	pF
Rg	Gate Resistance	V_{DS} = 15mV, f = 1MHz	0.1	3.1	6.2	Ω
Switching Characteristics						
t$_{d(on)}$	Turn-On Delay Time	V_{DD} = 50V, I_D = 4.4A V_{GS} = 10V, R_{GEN} = 24Ω		11	20	ns
t$_r$	Rise Time			25	40	ns
t$_{d(off)}$	Turn-Off Delay Time			35	56	ns
t$_f$	Fall Time			26	42	ns
Q$_g$	Total Gate Charge	V_{GS} = 10V V_{DD} = 50V I_D = 4.4A		13	17	nC
Q$_{gs}$	Gate to Source Gate Charge			3.6		nC
Q$_{gd}$	Gate to Drain "Miller" Charge			3.4		nC
Drain-Source Diode Characteristics						
V$_{SD}$	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 4.4A			1.25	V
		V_{GS} = 0V, I_S = 2.2A			1.0	V
t$_{rr}$	Reverse Recovery Time	I_F = 4.4A, di/dt = 100A/μs			56	ns
Q$_{rr}$	Reverse Recovery Charge				108	nC

Notes:
1: R$_{θJA}$ is determined with the device mounted on a 1 in^2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R$_{θJC}$ is guaranteed by design while R$_{θJA}$ is determined by the user's board design.
(a)R$_{θJA}$ = 60°C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5'x1.5'x0.062' thick PCB.
(b)R$_{θJA}$ = 135°C/W when mounted on a minimum pad of 2 oz copper.
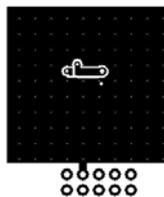
a. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 135°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.
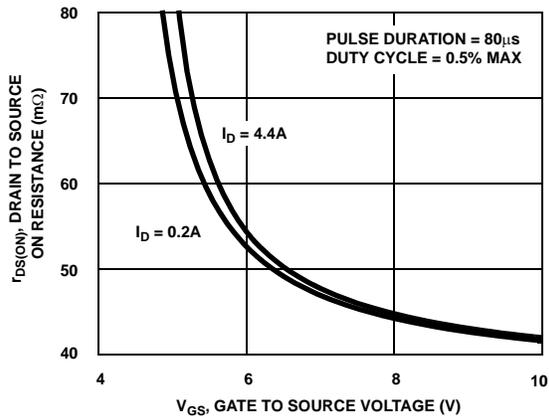**3:** E$_{AS}$ of 54 mJ is based on starting T$_J$ = 25 C; N-ch: L = 3 mH, I$_{AS}$ = 6 A, V$_{DD}$ = 100 V, V$_{GS}$= 10 V.

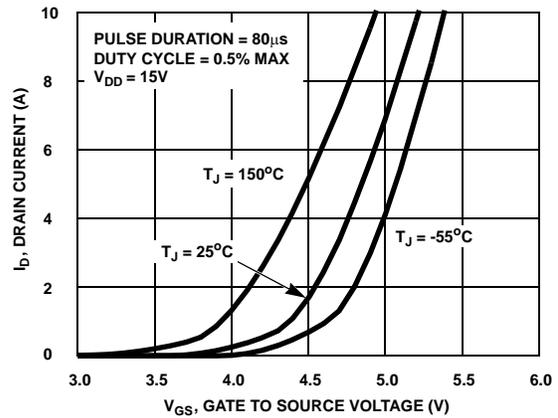## Typical Characteristics T_J = 25°C unless otherwise noted
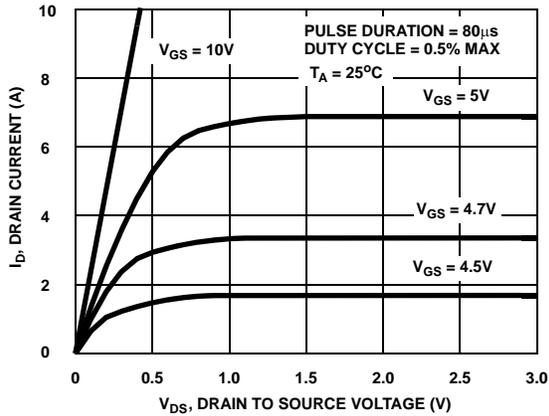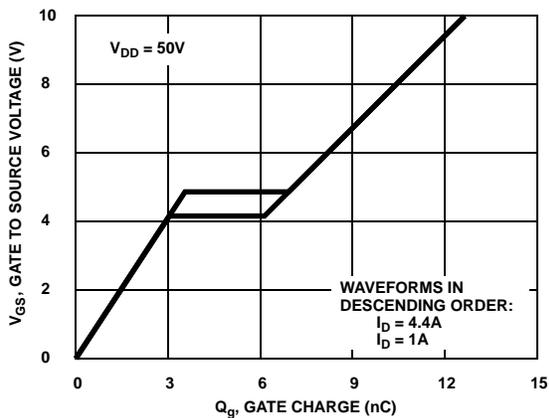
Figure 1. On-Region Characteristics
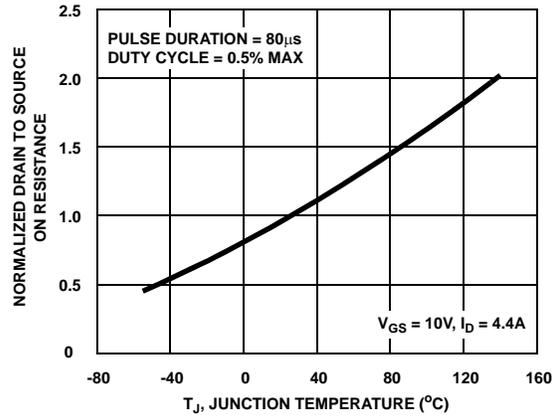
Figure 2. Normalized On-Resistance vs Junction Temperature
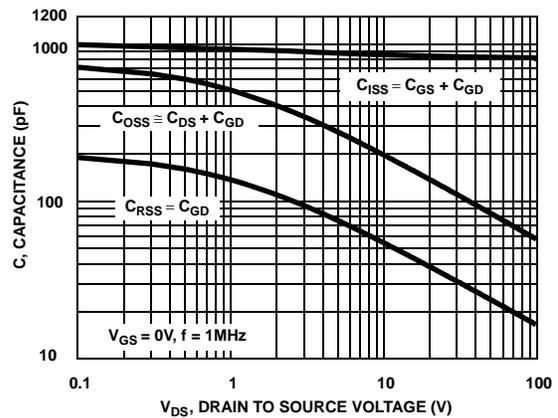
Figure 3. On-Resistance vs Gate to Source Voltage

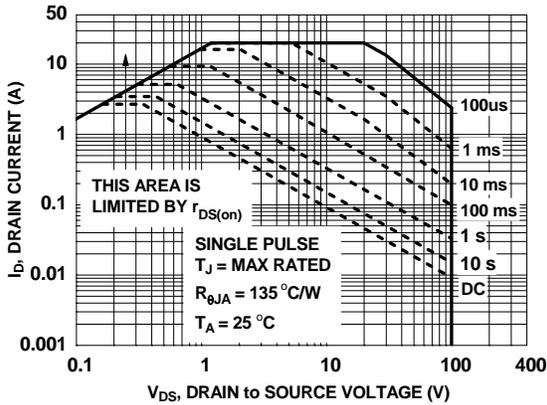**Figure 4. Transfer Characteristics**
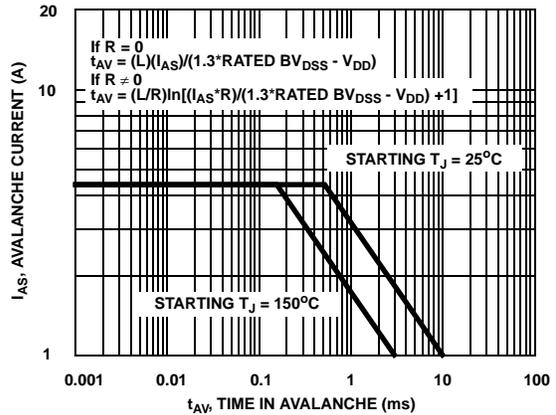
Figure 5. Gate Charge Characteristics

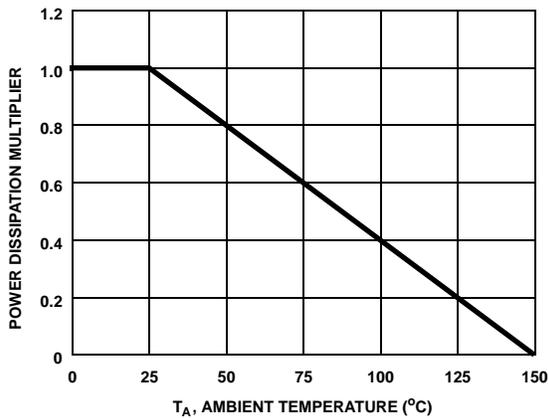**Figure 6. Capacitance vs Drain to Source Voltage**

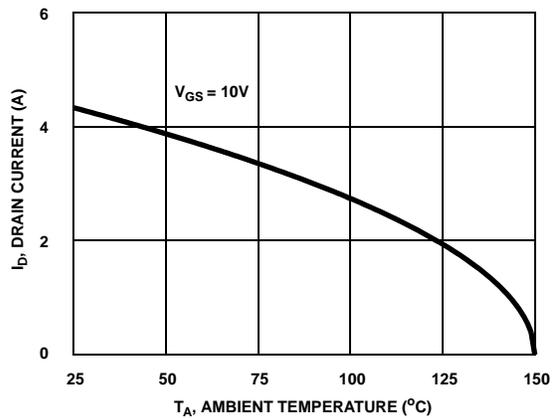## Typical Characteristics $T_J = 25°C$ unless otherwise noted
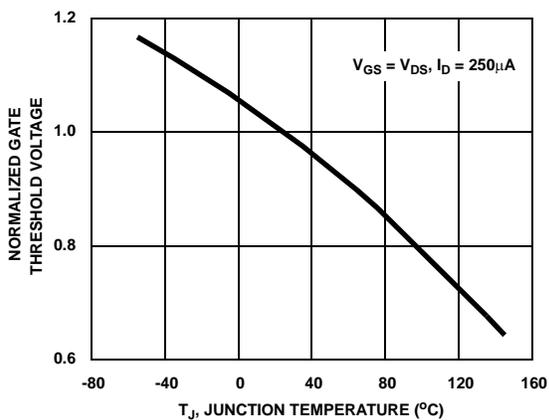

Figure 7. Forward Bias Safe Operating Area

Figure 8. Uncalamped Inductive Switching Capability

Figure 9. Normalized Power dissipation vs Ambient Temperature

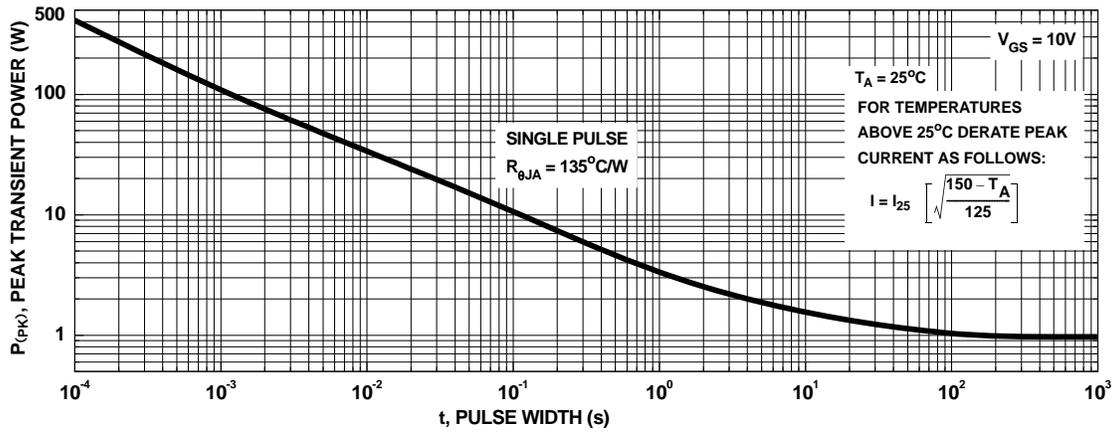**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

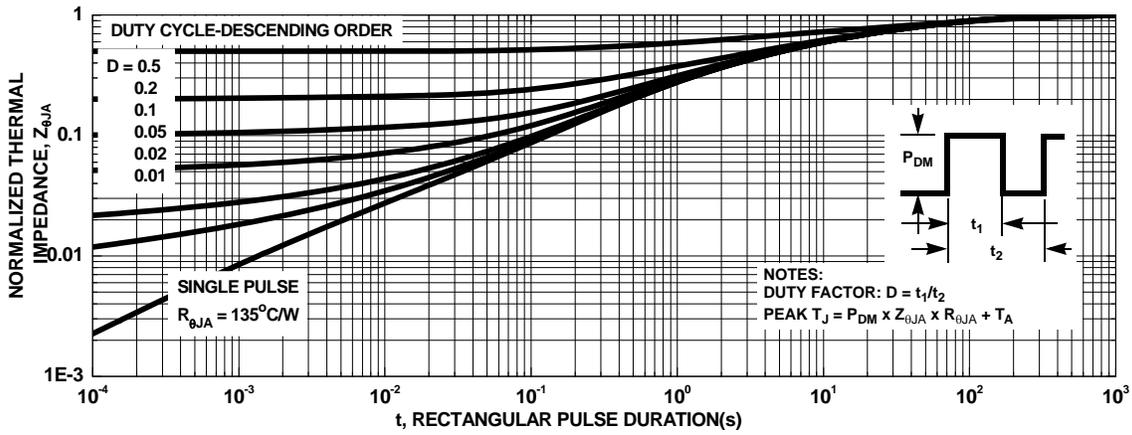**Figure 11. Normalized Gate Threshold voltage vs Junction Temperature**
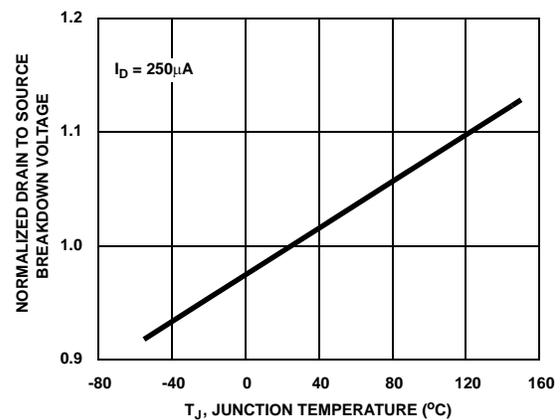
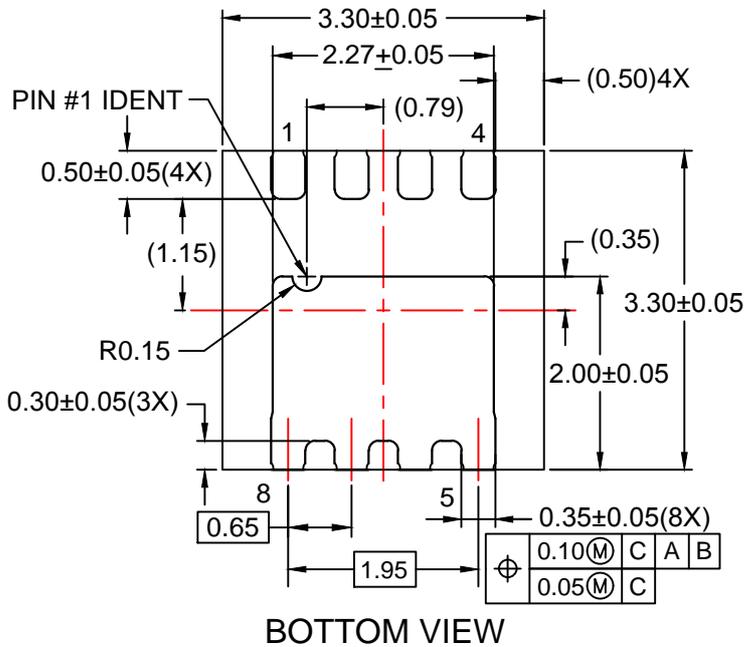**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**
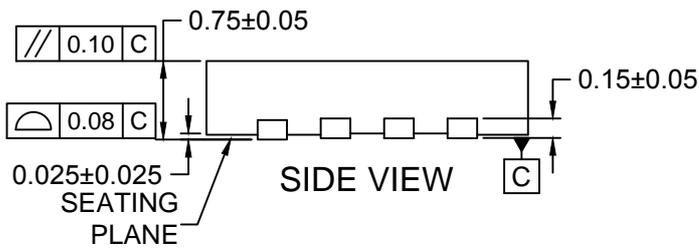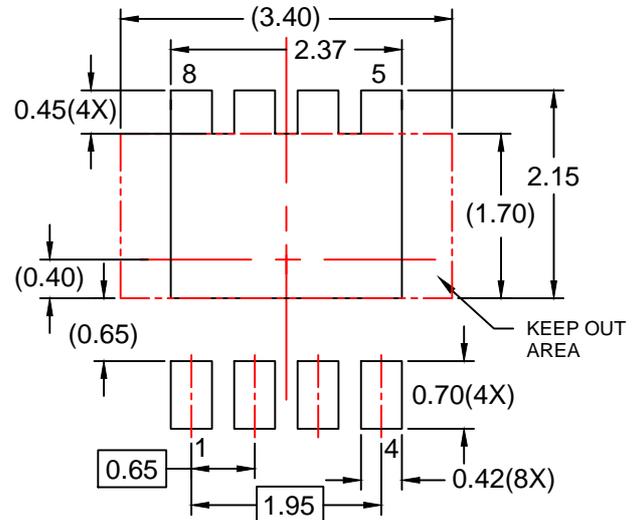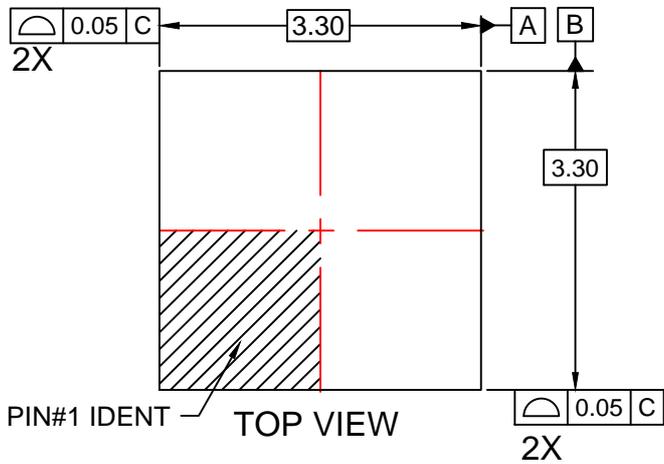
Typical Characteristics T_J = 25°C unless otherwise noted

V_{GS} = 10V

T_A = 25°C

FOR TEMPERATURES
ABOVE 25°C DERATE PEAK
CURRENT AS FOLLOWS:

$$I = I_{25} \left[\sqrt{\frac{150 - T_A}{125}} \right]$$

SINGLE PULSE

$R_{\theta JA}$ = 135°C/W

Figure 13. Peak Current Capability

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE
$R_{\theta JA}$ = 135°C/W

P_{DM}

t_1

t_2

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JA}$ x $R_{\theta JA}$ + T_A

Figure 14. Transient Thermal Response Curve

TOP VIEW

2X | ⌓ | 0.05 | C |

3.30

| A | B |

3.30

⌓ | 0.05 | C |
2X

PIN#1 IDENT

TOP VIEW

SIDE VIEW

∥ | 0.10 | C |

0.75±0.05

⌓ | 0.08 | C |

0.15±0.05

0.025±0.025
SEATING
PLANE

SIDE VIEW

| C |

BOTTOM VIEW

3.30±0.05

2.27±0.05

(0.50)4X

PIN #1 IDENT

(0.79)

0.50±0.05(4X)

1   4

(1.15)

(0.35)

R0.15

3.30±0.05

0.30±0.05(3X)

2.00±0.05

8   5

0.65

0.35±0.05(8X)

1.95

⌖ | 0.10 Ⓜ | C | A | B |

| 0.05 Ⓜ | C |

BOTTOM VIEW

RECOMMENDED LAND PATTERN

(3.40)

2.37

8   5

0.45(4X)

2.15

(1.70)

(0.40)

(0.65)

KEEP OUT
AREA

0.70(4X)

0.65   1   4   0.42(8X)

1.95

RECOMMENDED LAND PATTERN

NOTES:

A. DOES NOT CONFORM TO JEDEC
REGISTRATION MO-229

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS
EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP08Srev3.

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PUBLICATION ORDERING INFORMATION

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