LPC-P1343 development board
user's manual

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Revision C, February 2013
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INTRODUCTION

LPC-P1343 is a development board with LPC1343 ARM Cortex-M3 based microcontroller for embedded applications from NXP. LPC-P1343 featuring a high level of integration and low power consumption. This microcontroller supports various interfaces such as one Fast-mode Plus I²C-bus interface, USB, UART, SSP interfaces, four general purpose timers, a 10-bit ADC. On the board are available UEXT, Debug Interface, user buttons, USB device and user LEDs. This allows you to build a diversity of powerful software that can be used in a wide range of applications.

BOARD FEATURES

- MCU: **LPC1343** Cortex-M3, up to 70 MHz, 32 kB Flash, 8kB SRAM, UART RS-485, USB, SSP, I²C/Fast+, ADC

- Power supply circuit

- Power-on led

- USB connector and functionality

- USBC LED

- Debug interface – SWD (Serial Wire Debug)

- UEXT connector

- Eight user LEDs

- Two user buttons

- Reset button

- Prototype area

- FR-4, 1.5 mm, red soldermask, white component print

- Dimensions:80x50mm (3.15 x 1.97")

ELECTROSTATIC WARNING

The **LPC-P1343** board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

BOARD USE REQUIREMENTS

Cables: The cable you will need depends on the programmer/debugger you use. For instance, if you use https://www.olimex.com/Products/ARM/JTAG/ARM-JTAG-COOCOX/, you will need USB A-B cable.

Hardware: Programmer/debugger or other compatible programming/debugging tool with SWD interface. The only Olimex programmer that has SWD interface at the moment is ARM-JTAG-COOCOX – https://www.olimex.com/Products/ARM/JTAG/ARM-JTAG-COOCOX.

OpenOCD debuggers (ARM-JTAG-TINY, ARM-JTAG-TINY-H, ARM-JTAG-OCD, ARM-JTAG-OCD-H) can also be adapted to work with SWD interface by getting https://www.olimex.com/Products/ARM/JTAG/ARM-JTAG-SWD/. NOTE that at the current moment only Rowley Crossworks supports this combination.
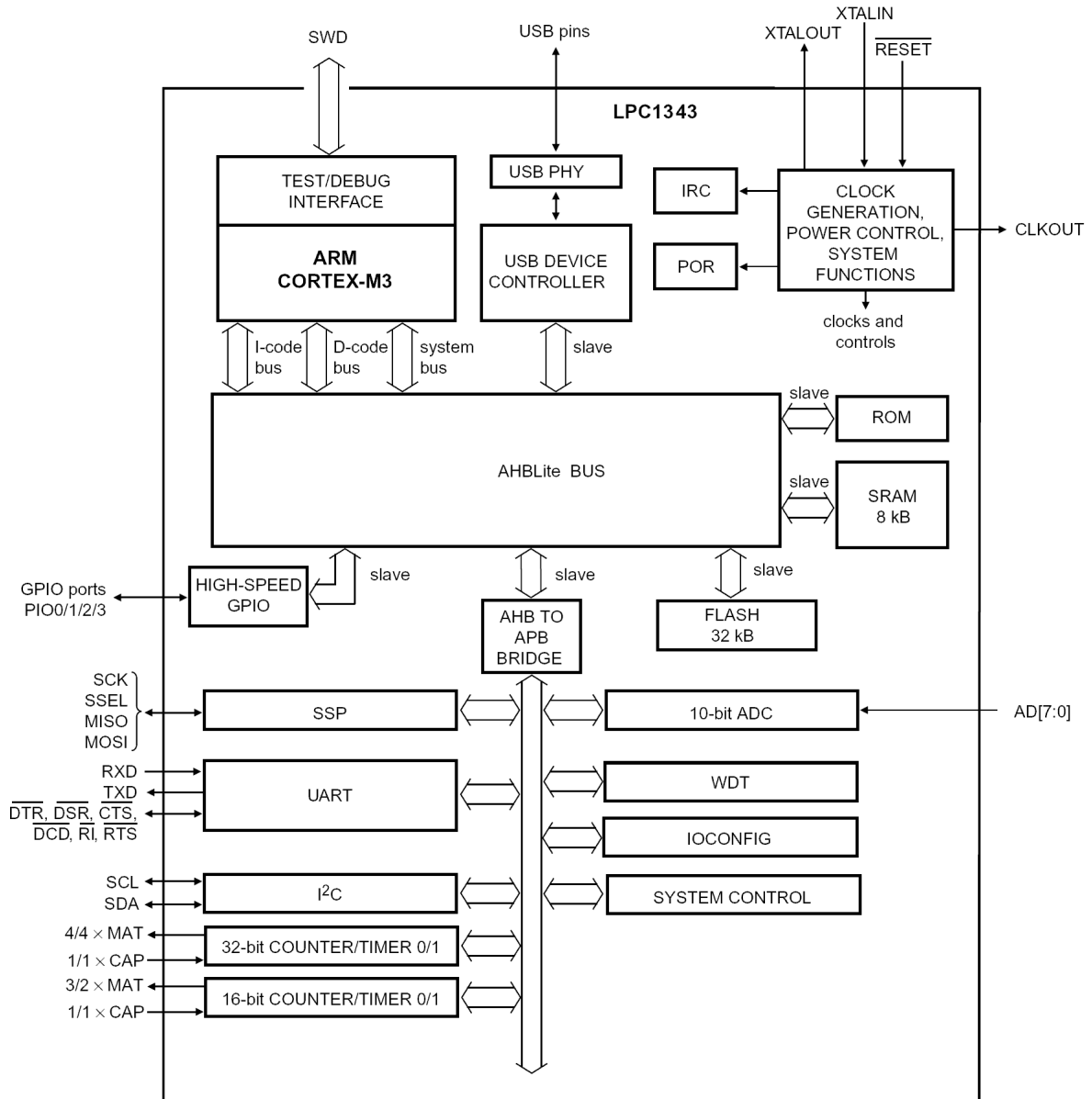
PROCESSOR FEATURES

LPC-P1343 board use ARM Cortex™-M3 microcontroller **LPC1343FBD48/301** from NXP Semiconductors with these features:
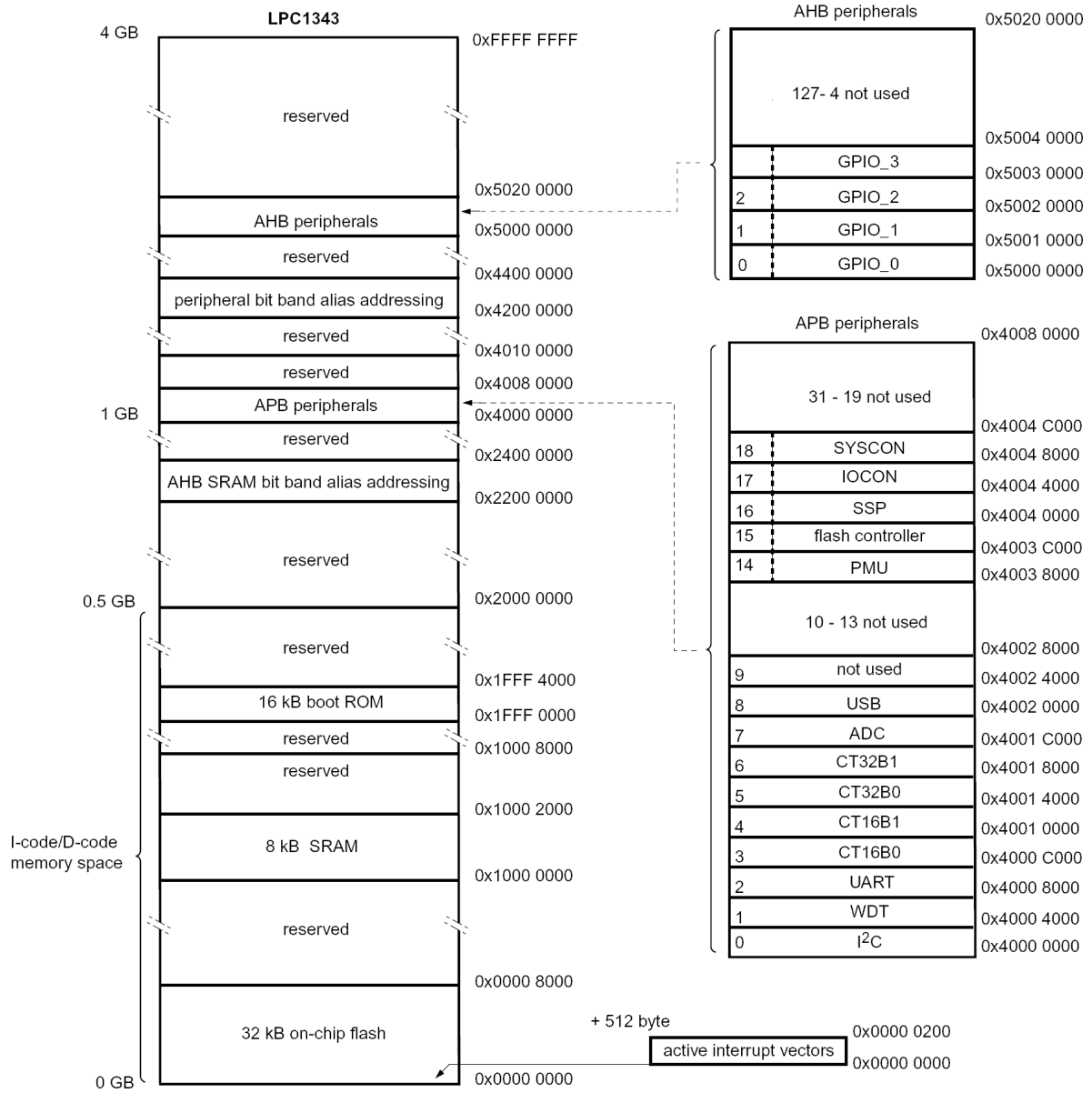
– ARM Cortex-M3 processor, running at frequencies of up to 72 MHz

– ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).

– 32kB on-chip flash programming memory. Enhanced flash memory accelerator enables high- peed 72 MHz operation with zero wait states

– In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.

– Serial interfaces:

   - USB 2.0 full-speed device controller with on-chip PHY for device

   - UART with fractional baud rate generation, modem, internal FIFO and RS-485/EIA-485 support.

   - SSP controller with FIFO and multi-protocol capabilities.

   - I²C-bus interface supporting full I²C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.

– Other peripherals:

   - 42 General Purpose I/O (GPIO) pins with configurable pull-up/down resistors and a new, configurable open-drain operating mode.

   - Four general purpose timers/counters, with a total of four capture inputs and 13 match outputs.

        - Programmable WatchDog Timer (WDT).

        - System tick timer.

– Serial Wire Debug and Serial Wire Trace Port.

– High-current output driver (20 mA) on one pin.

– High-current sink drivers (20 mA) on two I2C-bus pins in Fast-mode Plus.

– Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.

– Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.

– Single 3.3 V power supply (2.0 V to 3.6 V).

– 10-bit ADC with input multiplexing among 8 pins.

– 40 GPIO pins can be used as edge and level sensitive interrupt sources.

– Clock output function with divider that can reflect the main oscillator clock, IRC clock, CPU clock, Watchdog clock, and the USB clock.

– Processor wake-up from Deep-sleep mode via GPIO interrupts.

– Brownout detect with four separate thresholds for interrupt and one threshold for forced reset.

– Power-On Reset (POR).

– Crystal oscillator with an operating range of 1 MHz to 25 MHz.

– 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.

– PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the Watchdog oscillator.

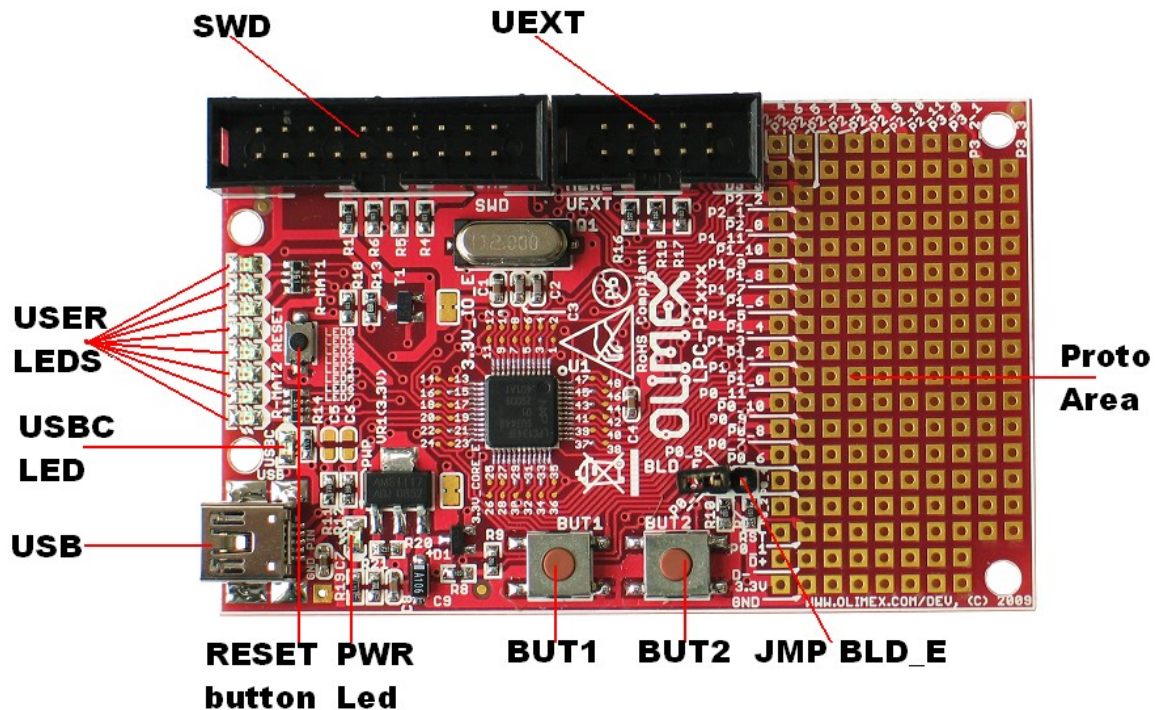– Code Read Protection (CRP) with different security levels.

BLOCK DIAGRAM

MEMORY MAP

LPC1343

4 GB		0xFFFF FFFF

reserved

0x5020 0000

AHB peripherals
0x5000 0000

reserved
0x4400 0000

peripheral bit band alias addressing
0x4200 0000

reserved
0x4010 0000

reserved
0x4008 0000

1 GB — APB peripherals
0x4000 0000

reserved
0x2400 0000

AHB SRAM bit band alias addressing
0x2200 0000

reserved
0x2000 0000

0.5 GB

reserved
0x1FFF 4000

16 kB boot ROM
0x1FFF 0000

reserved
0x1000 8000

reserved
0x1000 2000

8 kB SRAM
0x1000 0000

reserved

0x0000 8000

32 kB on-chip flash
0x0000 0000

0 GB

I-code/D-code memory space

AHB peripherals   0x5020 0000

127- 4 not used

0x5004 0000

	GPIO_3	0x5003 0000
2	GPIO_2	0x5002 0000
1	GPIO_1	0x5001 0000
0	GPIO_0	0x5000 0000

APB peripherals   0x4008 0000

31 - 19 not used

0x4004 C000

18	SYSCON	0x4004 8000
17	IOCON	0x4004 4000
16	SSP	0x4004 0000
15	flash controller	0x4003 C000
14	PMU	0x4003 8000

10 - 13 not used

0x4002 8000

9	not used	0x4002 4000
8	USB	0x4002 0000
7	ADC	0x4001 C000
6	CT32B1	0x4001 8000
5	CT32B0	0x4001 4000
4	CT16B1	0x4001 0000
3	CT16B0	0x4000 C000
2	UART	0x4000 8000
1	WDT	0x4000 4000
0	I^{2}C	0x4000 0000

+ 512 byte

active interrupt vectors   0x0000 0200
0x0000 0000

SCHEMATIC

LPC-P1343

Rev. Initial

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http://www.olimex.com/dev

DEBUG INTERFACE:

UEXT

BUTTONS

POWER SUPPLY

U1 LPC1343FBD48

BOARD LAYOUT

POWER SUPPLY CIRCUIT

LPC-P1343 is power supplied +5V via USB, or via JTAG.

RESET CIRCUIT

LPC-P1343 reset circuit includes LPC1343 pin 3 (#RESET/PIO0_0), R18 (10k) and RESET button.

CLOCK CIRCUIT

Quartz crystal 12 MHz is connected to LPC1343 pin 6 (XTALIN) and pin 7 (XTALOUT).

JUMPER DESCRIPTION

3.3V_CORE_E

This jumper, when closed, enables microcontroller 3.3V power supply.
Default state is closed.

3.3V(I/O)_E

This jumper, when closed, supplies 3.3 V voltage to LPC1343 pin 8 (VDDIO).
Default state is closed.

BLD_E

If BLD_E is closed during Reset and USB is connected to computer, then removable disk will appear in My computer. The user can create via IAR "*.bin" file, which can be placed into the removable disk. After this when you open jumper BLD_E and then reset the board the microcontroller will execute the program stored in the "*.bin" file. <u>Default state is open.</u>

INPUT/OUTPUT

LED0 (red) connected via R-MAT1 to LPC1343 pin 36 (PIO3_0).

LED1 (red) connected via R-MAT1 to LPC1343 pin 37 (PIO3_1).

LED2 (red) connected via R-MAT1 to LPC1343 pin 43 (PIO3_2).

LED3 (red) connected via R-MAT1 to LPC1343 pin 48 (PIO3_3).

LED4 (red) connected via R-MAT2 to LPC1343 pin 18 (PIO2_4).

LED5 (red) connected via R-MAT2 to LPC1343 pin 21 (PIO2_5).

LED6 (red) connected via R-MAT2 to LPC1343 pin 1 (PIO2_6).

LED7 (red) connected via R-MAT2 to LPC1343 pin 11 (PIO2_7).

USBC (yellow) shows that USB is connected.

Power-on LED (red) – this LED shows that +3.3V is applied to the board.

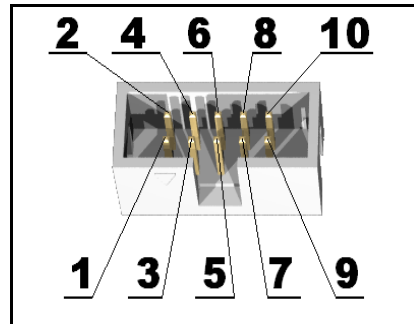**User button** with name **BUT1** (USER) connected to **LPC1343** pin 24 (PIO2_9).

User button with name **BUT2** connected to **LPC1343** pin 40 (WAKEUP).

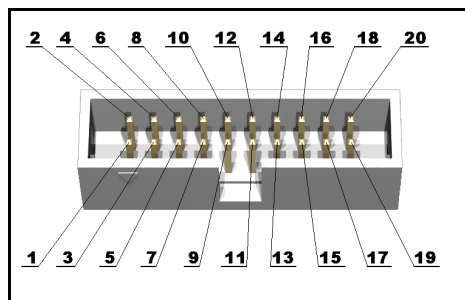**Reset button** with name **RESET** connected to **LPC1343** pin 3 (#RESET/PIO0_0).

EXTERNAL CONNECTORS DESCRIPTION

UEXT

Pin #	Signal Name
1	3.3V
2	GND
3	TXD
4	RXD
5	SCL
6	SDA
7	MISO
8	MOSI/SWV
9	SCK
10	CS

SWD

Pin #	Signal Name	Pin #	Signal Name
1	3.3V	2	3.3V
3	NC	4	GND
5	NC	6	GND
7	SWD	8	GND
9	SWC	10	GND
11	pull-down	12	GND
13	MOSI/SWV	14	GND
15	NC	16	GND
17	pull-down	18	GND
19	+5V_JLINK	20	GND

USB

Pin #	Signal Name
1	USB_VBUS
2	U2D-
3	U2D+
4	NC
5	GND
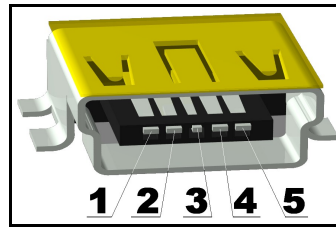
MECHANICAL DIMENSIONS
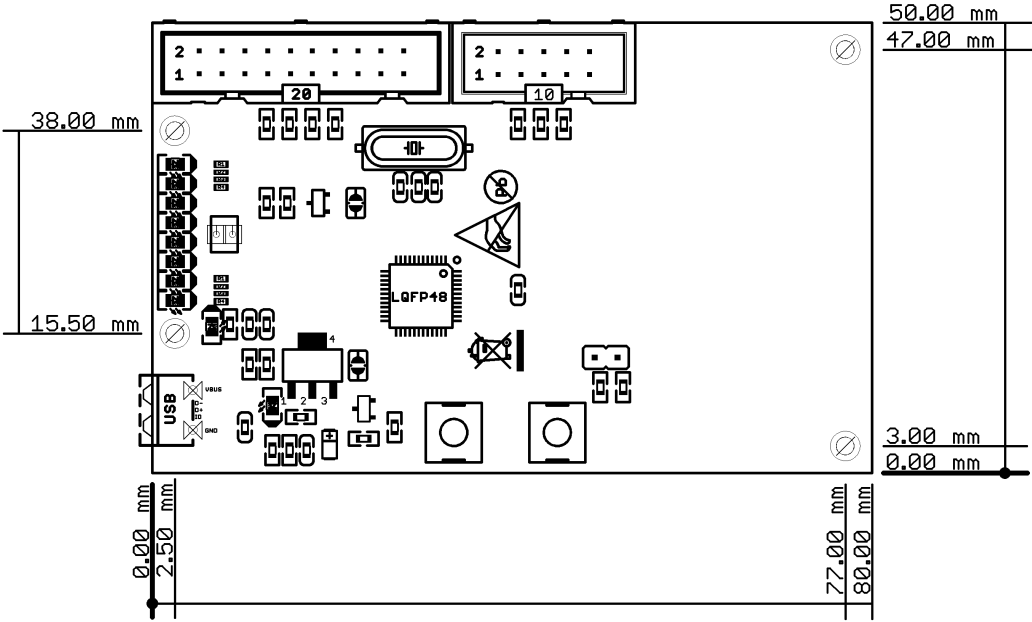
AVAILABLE DEMO SOFTWARE

- [LPC1343 demo examples](#) project for EW-ARM

ORDER CODE

LPC-P1343 - assembled and tested board

How to order?

You can order directly from our web shop or by any of our distributors. The list of distributors may be found here: https://www.olimex.com/Distributors/

Check our web site https://www.olimex.com/ for more info.

Revision history

Revision Initial, December 2009

Revision A, February 2011 – available demo software added

Revision B, May 2012 – fixed errors on page 9 regarding LED4 and LED5 processor pins

Revision C, February 2013 – updated links, disclaimer and suggested debuggers

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The software is released under GPL.

It is possible that the pictures in this manual differ from the latest revision of the board.

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