



PHY1076-01 125Mbps to 2.7Gbps Laser Driver/ Post Amp with Digital Diagnostics

Features

- Multi-rate from 125Mbps to 2.7Gbps
- Laser driver output stage with 70mA max modulation drive and 100mA bias current
- Programmable mean power control loop
- Temperature compensated modulation current
- Integrated limiting amplifier with selectable swing CML output
- Programmable receiver low pass filter
- Integrated Loss Of Signal function
- Digital diagnostic mode compliant with SFF-8472 using an external MCU
- Stand-alone mode where device parameters are loaded from an external EEPROM
- -40°C to +95°C ambient operating range
- 36pin 6mm x 6mm QFN package
- Eye safety logic

Applications

Fibre Channel 1x, 2x
Gigabit Ethernet, SONET/SDH
OC-3, OC-12, OC-48

Description

The PHY1076-01 is a combined Laser driver and limiting amplifier with support for Digital Diagnostic Monitoring for use within small form factor modules for Fibre Channel, GbE and SONET/SDH applications.

The transmitter integrates a high speed output stage with programmable bias and modulation currents, controlled through a 2-wire serial interface. The mean power control loop allows connection in common anode configuration.

A Loss Of Signal (LOS) detector is included with detection based on either the receiver photo detector average current or received signal modulation amplitude.

When used in digital diagnostics mode the integrated A/D converters measuring temperature, TX Bias, Supply Voltage, RX Signal Strength and Mean Power are read via a 2-wire serial interface. An external Microcontroller Unit (MCU) is used for calibrating real time diagnostic monitors and alarm generation.

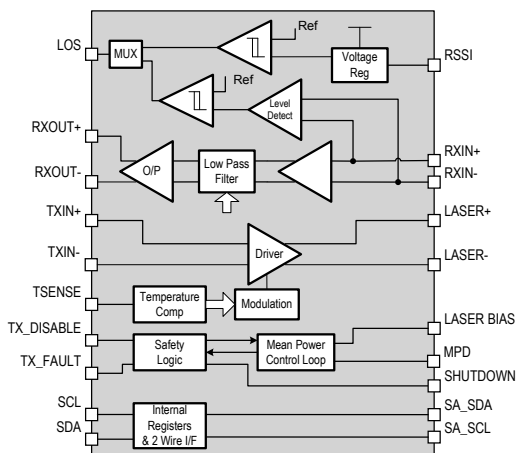


Figure 1 - Outline Block Diagram

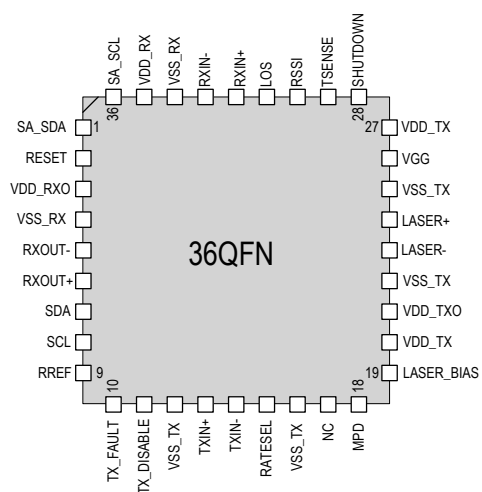


Figure 2 - Device Pin Out (Top View)

Table of Contents

| | | |
|------|---|----|
| 1. | Ordering Information | 3 |
| 2. | Pin Description | 3 |
| 3. | Key Specifications..... | 5 |
| 3.1. | Absolute Maximum Ratings | 5 |
| 3.2. | Continuous Ratings..... | 5 |
| 3.3. | Receiver | 5 |
| 3.4. | Transmitter | 7 |
| 3.5. | 2-Wire Serial Interface | 10 |
| 3.6. | Typical Operating Characteristics | 12 |
| 4. | Functional Description | 13 |
| 4.1. | Overview | 13 |
| 4.2. | Receiver Features..... | 14 |
| 4.3. | Transmitter Features..... | 17 |
| 4.4. | Laser Safety Features..... | 19 |
| 4.5. | Tsense Temperature Sensor | 21 |
| 5. | Control Interface | 22 |
| 5.1. | Memory Map | 22 |
| 5.2. | Operation..... | 23 |
| 5.3. | Digital Diagnostics Mode..... | 28 |
| 5.4. | Stand-Alone Mode | 30 |
| 5.5. | 2-wire Serial Interface | 32 |
| 6. | Register Map..... | 34 |
| 7. | Simplified Interface Models..... | 43 |
| 8. | Typical Applications | 45 |
| 8.1. | Power Supply Connections..... | 46 |
| 9. | Packaging | 48 |
| 10. | Contact Information..... | 49 |

1. Ordering Information

Please refer to the Packaging section for test and package location ordering code definitions.

| Part Number | Description | Package |
|---|---|---|
| PHY1076-01QD-RR | Enhanced 2.7G LASER driver and Post Amp | QFN36, 6mmx6mm in Tape and Reel, RoHS compliant (see Figure 41) |
| PHY1076-01QS-RR NOT FOR USE IN NEW DESIGNS | Enhanced 2.7G LASER driver and Post Amp | QFN36, 6mmx6mm in Tape and Reel, RoHS (see Figure 41) |

2. Pin Description

| Pin No | Name | Direction | Type | Description |
|--------|-------------------------|-----------|----------------------------|---|
| 1 | SA_SDA ^{1,4} | I/O | LVTTTL | 2-wire serial interface. Connects to EEPROM in stand-alone mode |
| 2 | RESET | I/P | CMOS | Reset |
| 3 | VDD_RXO ² | | Power | Limiting amplifier output power supply |
| 4 | VSS_RX ³ | | Ground | Receiver section ground connection |
| 5 | RXOUT- | O/P | CML | Limiting amplifier differential serial data output. |
| 6 | RXOUT+ | O/P | CML | Limiting amplifier differential serial data output. |
| 7 | SDA ⁴ | I/O | LVTTTL | 2-wire serial data interface. Used in Digital Diagnostics Mode. |
| 8 | SCL ⁴ | I/P | LVTTTL | 2-wire serial interface clock. Used in Digital Diagnostics Mode. |
| 9 | RREF | I/P | Analog | Connect to Ground through a 10k resistor |
| 10 | TX_FAULT | O/P | LVTTTL (open collector) | Transmit fail alarm. A logic 1 indicates a fault in the transmission system. Requires external pull up for SFP MSA compliance |
| 11 | TX_DISABLE ⁴ | I/P | LVTTTL | Output disable (active high). Disables Laser drive. On chip 8k pull up |
| 12 | VSS_TX ³ | | Ground | Transmission circuitry ground connection |
| 13 | TXIN+ | I/P | CML | Differential Laser driver input from host |
| 14 | TXIN- | I/P | CML | Differential Laser driver input from host |
| 15 | RATESEL | I/P | LVTTTL | Toggles between two low pass filter characteristics. External 30k pull down resistor required for SFP MSA compliance |
| 16 | VSS_TX ³ | | Ground | Transmission circuitry ground connection |
| 17 | NC | | | No connection. Leave open circuit |
| 18 | MPD | I/P | Analog | Monitor photodiode input |
| 19 | LASER_BIAS | O/P | Analog | Laser bias current output |
| 20 | VDD_TX ² | | Power | Transmission circuitry power supply connection |
| 21 | VDD_TXO ² | | Power | Transmission circuitry power supply connection |
| 22 | VSS_TX ³ | | Ground | Transmission circuitry ground connection |
| 23 | LASER- | O/P | High speed | Laser differential driver output |

| | | | | |
|----|-----------------------|-----|----------------------------|---|
| 24 | LASER+ | O/P | High speed | Laser differential driver output |
| 25 | VSS_TX ³ | | Ground | Transmission circuitry ground connection |
| 26 | VGG | | Ground | Ground substrate connection |
| 27 | VDD_TX ² | | Power | Transmission circuitry power supply connection |
| 28 | SHUTDOWN | O/P | CMOS | Gate drive for optional Laser shutdown FET switch |
| 29 | TSENSE | I/P | Analog | External temperature sensing transistor connection |
| 30 | RSSI | I/P | Analog | Receive signal strength indicator & regulated supply for Rx photodiode |
| 31 | LOS | O/P | LVTTTL (open collector) | Loss of signal output. Requires external pull up for SFP MSA compliance |
| 32 | RXIN+ | I/P | CML | Limiting amplifier differential serial data input |
| 33 | RXIN- | I/P | CML | Limiting amplifier differential serial data input |
| 34 | VSS_RX ³ | | Ground | Receiver ground connection |
| 35 | VDD_RX ² | | Power | Limiting amp power supply |
| 36 | SA_SCL ^{1,4} | I/P | LVTTTL | EEPROM 2-wire serial interface clock |
| - | PADDLE | | Ground | Ground / Thermal Paddle |

1 Used in stand-alone mode only

2 All VDDs are internally connected by back-to-back protection diodes. VDDs should not be powered up independently.

3 All VSSs are internally connected to the IC substrate connection.

4 Internally pulled high with an 8kΩ pull-up resistor.

3. Key Specifications

3.1. Absolute Maximum Ratings

| Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|------------------|-----------|-----|-----------|------|
| Supply Voltage | | - 0.5 | | +6.5 | V |
| Voltage on any pin | | VSS - 0.5 | | VDD + 0.5 | V |
| Storage Temperature | | | | 150 | °C |
| Soldering Temperature | For 25 seconds | | | 260 | °C |
| Junction Temperature | | | | 140 | °C |
| ESD | Human Body Model | 2 | | | kV |

Under absolute maximum rating conditions device not guaranteed to meet specifications; permanent damage may be incurred by operating beyond these limits.

3.2. Continuous Ratings

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|------|-----|------------|------|
| Operating Supply Voltage | Continuous operation | 2.97 | 3.3 | 3.63 | V |
| Current consumption | $I_{dd} = I_{ddo} + (K_m \cdot I_{mod}) + (K_b \cdot I_{bias})$ | | | | mA |
| Current Consumption (I _{ddo}) | High Swing, OMA LOS, V _{ref} = 113 2448Mbps Filter 155Mbps Filter | | | 118 110 | mA |
| Current consumption (K _m) | | | | 0.536 | |
| Current consumption (K _b) | | | | 0.075 | |
| Operating temperature | Ambient Still Air, Max Bias and Modulation Current | -40 | 25 | +95 | °C |

3.3. Receiver

3.3.1. Receive Limiting Amplifier

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|------------------------------|--------|---|------------|-----|-------------|--------|
| Sensitivity | | Differential, BER=1*10 ⁻¹² (125 - 2.125Gbps) | | 5 | 7.5 | mVpp |
| Max Differential Input | | TJ within spec | 1200 | | | mVpp |
| Input Return Loss | | Differential, f<2GHz, device powered on | | 10 | | dB |
| Output Return Loss | | Differential, f<2GHz, device powered on | | 10 | | dB |
| Low Frequency Cutoff | | High pass 3dB point for RX system | | 15 | | kHz |
| Differential Output Swing | | High swing mode Low swing mode | 800 400 | | 1100 520 | mVpp |
| Total Jitter, T _j | | Measured over RX input voltage range 125Mbps - 2.7Gbps | | | 100 | mUI pp |
| Duty Cycle Distortion | | 125Mbps - 2.7Gbps | 40 | | 60 | % |
| Output Resistance | | RXOUT+/- Single ended to VDD_RXO | 40 | 50 | 60 | Ω |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | | |
|--------------------------------------|-----------|---|---|--|-----|----------|-----|----|
| Input Impedance | | Differential RXIN+ to RXIN-, DC | 85 | | 115 | Ω | | |
| Rate select change time | t_ratesel | Using RATESEL pin | | | 5 | μ s | | |
| Output Rise and Fall Times (20%-80%) | | 155 Mbps filter, slow CMLslew = '1', low swing | | 200 | 300 | ps | | |
| | | 155 Mbps filter, fast CMLslew = '0', low swing | | 192 | 300 | | | |
| | | 155 Mbps filter, slow CMLslew = '1', high swing | | 261 | 400 | ps | | |
| | | 155 Mbps filter, fast CMLslew = '0', high swing | | 253 | 400 | | | |
| | | | 2488 Mbps filter, slow CMLslew = '1', low swing | | 71 | 100 | ps | |
| | | | 2488 Mbps filter, fast CMLslew = '0', low swing | | 63 | 90 | | |
| | | | | 2488 Mbps filter, slow CMLslew = '1', high swing | | 96 | 120 | ps |
| | | | | 2488 Mbps filter, fast CMLslew = '0', high swing | | 83 | 110 | |

3.3.2. RSSI Indicator and Rx PD Regulator

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------------------------|--------|---|-----|-----|------|---------|
| Voltage on RSSI pin | | Ireg=2mA (10nF & 100 Ω minimum load) | 2.4 | | | V |
| Current sourced by RSSI pin | | Measured using Rx Power ADC | 0 | | 2000 | μ A |

3.3.3. Receive Photocurrent LOS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-----------------------------|--------|--|-----|-----|-----|---------|
| RSSI LOS assert time | | | | | 10 | μ s |
| RSSI LOS de-assert time | | | | | 40 | μ s |
| Electrical Hysteresis | | $20\log_{10}(\text{RSSIdeassert} / \text{RSSIassert})$ | 2 | | 4 | dB |
| RSSI LOS assert level range | | Set by AVG_LOS_set, Address F4h | 4.0 | | 411 | μ A |

3.3.4. OMA LOS

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|------------------------|------------|--|-----|-----|-----|---------|
| OMA LOS assert time | t_loss_on | | | | 100 | μ s |
| OMA LOS de-assert time | t_loss_off | | | | 20 | μ s |
| Electrical Hysteresis | | $20\log_{10}(V\text{deassert} / V\text{assert})$ | 2.5 | | 5.5 | dB |
| OMA LOS assert level | | Set by OMA_LOS_set, Address F3h | 10 | | 50 | mV |

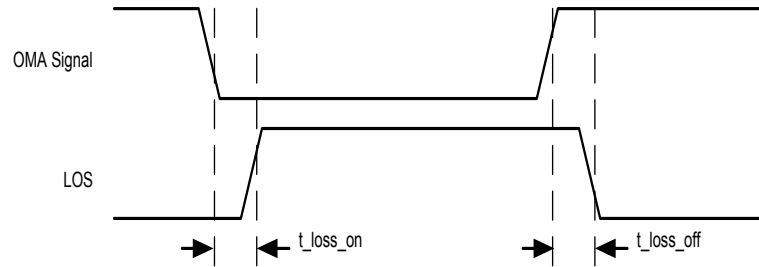


Figure 3 - OMA LOS Detection

3.4. Transmitter

3.4.1. Transmitter Inputs

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|--------|---|-----|-----|------|----------|
| High-Speed Data Input Signal Voltage ¹ | | Differential, AC-coupled, from 125Mbps to 2.7Gbps | 200 | | 2400 | mVpp |
| High-Speed Data Input Impedance | | Differential, DC | 80 | 100 | 120 | Ω |
| Input Return Loss | | Differential, $f < 2\text{GHz}$, device powered on | | 10 | | dB |
| Input common mode return loss | | Both inputs shorted together, measured using 25Ω source termination, 100MHz – 2.5GHz | | 10 | | dB |

3.4.2. Laser Driver

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|------------------|---|-----|-----|-----|--------|
| Modulation Current | I_{mod} | | 7 | | 70 | mA |
| Electrical 20% to 80% rise / fall time | | Measured using 50Ω effective termination, AC and DC coupled applications | | 55 | 65 | ps |
| Total Jitter contribution | | Measured over modulation current range | | | 100 | mUI pp |
| Laser output compliance range | | Allowed voltage for Laser driver output pins in dynamic operation, referenced to ground (VSS_TX). | 600 | | | mV |
| Bias current output compliance | | Minimum allowed voltage for pin LASER_BIAS, referenced to ground (VSS_TX) | 300 | | | mV |

3.4.3. Laser Mean Power Control Loop

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------|-----------------------|-----------------------------------|-----|----------|-----|---------------------|
| Bias Current | | | 0.5 | | 100 | mA |
| Bias current off | | Transmitter disabled | | | 10 | μA |
| Max current at MPD pin | | Sink current | | | 2.6 | mA |
| Turn on/off overshoot | | Bias current overshoot, Loop_BW=1 | | | 15 | % |
| APC -3dB Loop Bandwidth | $f_{\text{Loop_BW}}$ | Loop_BW = "0" Loop_BW = "1" | | 5 15 | | kHz |
| Bias loop settling time | t_{settle} | Loop_BW = "0" Loop_BW = "1" | | 5 500 | | ms μs |

3.4.4. Eye Safety Internal Fixed Limits

Operation outside these limits causes a TX_FAULT to be asserted

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|-------------|---|------|-----|------|------|
| High supply voltage assert limit | V_{eyeHa} | | 3.75 | | 4.10 | V |
| High supply voltage de-assert limit | V_{eyeHd} | | 3.65 | | 4.05 | V |
| High Supply Hysteresis | | | 0.05 | | 0.15 | V |
| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
| Low supply voltage assert limit | V_{eyeLa} | | 2.70 | | 2.95 | V |
| Low supply voltage de-assert limit | V_{eyeLd} | | 2.75 | | 2.95 | V |
| Low Supply Hysteresis | | | 0.01 | | 0.15 | V |
| RREF pin voltage limit | | RREF voltage applied to pin after calibration | 0.9 | | 1.1 | V |

3.4.5. Fault Timing

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|-----------------------------|-----------------|--|-----|-----|-----|---------|
| Time to initialize | t_{init} | From power on or application of $V_{cc} > 2.97V$ during plug in | | | 300 | ms |
| Hard TX_DISABLE assert time | t_{off} | Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal | | | 2 | μs |
| Hard TX_DISABLE negate time | t_{on} | Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal | | | 800 | μs |
| Hard TX_FAULT assert time | t_{fault} | Time from fault to TX_FAULT on | | | 100 | μs |
| TX_DISABLE pulse width | t_{reset} | Time TX_DISABLE must be held high to reset TX_FAULT | 5 | | | μs |
| TX_FAULT deassert time | $t_{faultdass}$ | Time to deassert TX_FAULT after TX_DISABLE | | | 300 | ms |

3.4.6. Diagnostic Timing Diagrams

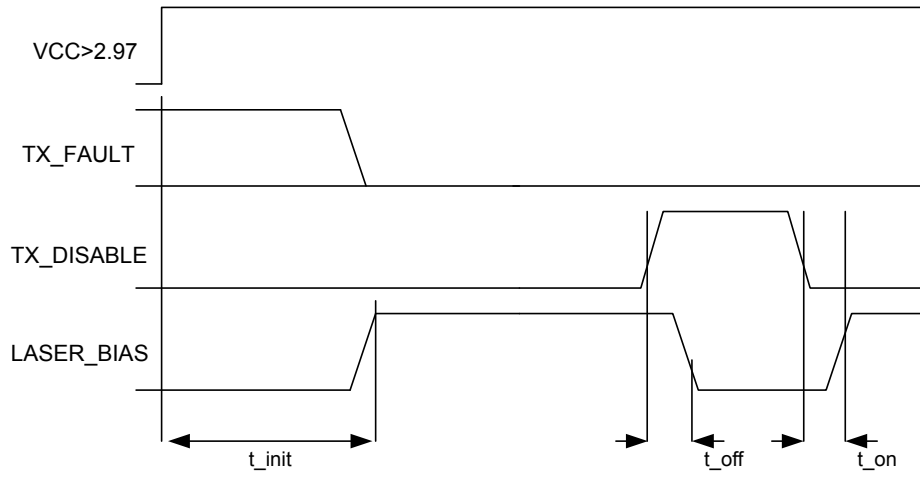


Figure 4 - Device turn on

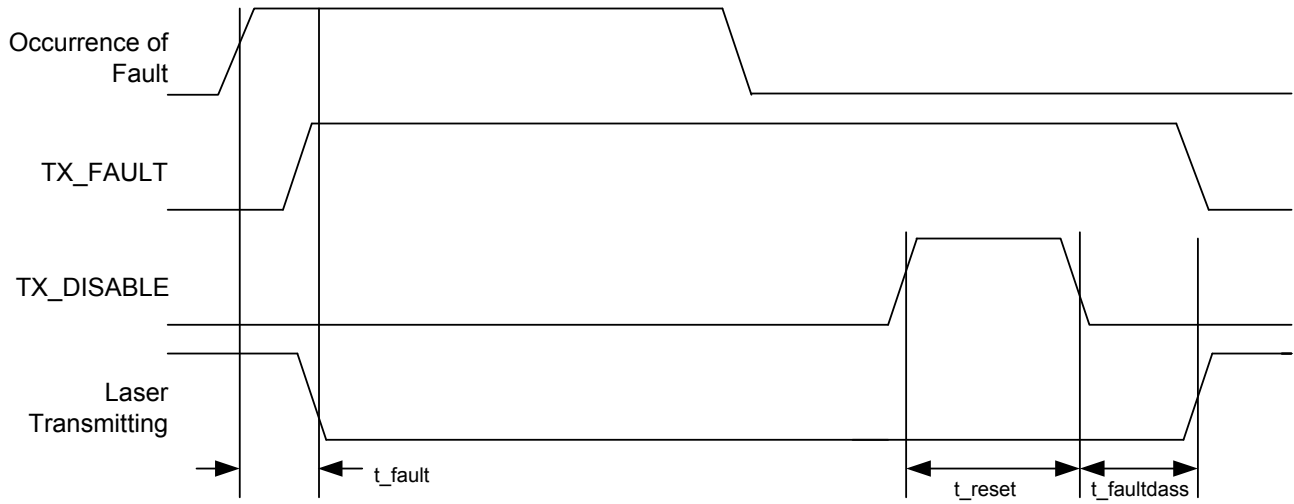


Figure 5 - Fault detection

3.5. 2-Wire Serial Interface

3.5.1. AC Electrical Characteristics

| Parameter | Symbol | Comment | Min | Typ | Max | Unit |
|--|--------------|---------------------------------------|-----|-----|------|---------|
| SCL clock frequency | f_{SCL} | | 0 | | 100 | kHz |
| LOW period of the SCL clock | t_{LOW} | | 4.7 | | – | μ s |
| HIGH period of the SCL clock | t_{HIGH} | | 4.0 | | – | μ s |
| Set-up time for a repeated START condition | $t_{SU:STA}$ | | 4.7 | | – | μ s |
| Hold time (repeated) START condition | $t_{HD:STA}$ | | 4.0 | | – | μ s |
| Data hold time | $t_{HD:DAT}$ | | 0 | | 3.45 | μ s |
| Data set-up time | $t_{SU:DAT}$ | | 250 | | – | ns |
| Rise time of both SDA and SCL signals | t_R | | – | | 1000 | ns |
| Fall time of both SDA and SCL signals | t_F | | – | | 300 | ns |
| Set-up time for STOP condition | $t_{SU:STO}$ | | 4.0 | | – | μ s |
| Bus free time between a STOP and START condition | t_{BUF} | | 4.7 | | – | μ s |
| Output fall time from VIHmin to VILmax | t_{of} | $10\text{pF} < C_b(1) < 400\text{pF}$ | 0 | | 250 | ns |
| Capacitance for each I/O pin | C_i | See note 1 | – | | 10 | pF |

1 C_b = capacitance of a single bus line in pF.

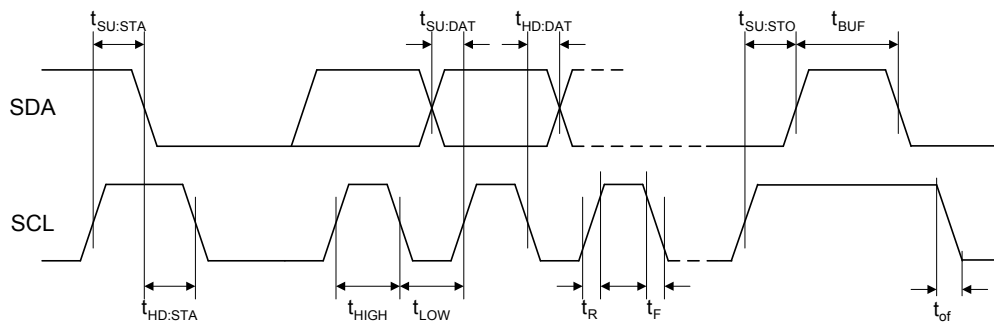


Figure 6 - SDA and SCL bus timing

3.5.2. DC Electrical Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|--------------------------|----------|-------------------------------|--------------|-----|----------------|------|
| Low level input voltage | V_{IL} | | - 0.5 | | $0.3 V_{DD}$ | V |
| High level input voltage | V_{IH} | | $0.7 V_{DD}$ | | $V_{DD} + 0.5$ | V |
| Low level O/P voltage | V_{OL} | 3 mA sink current | 0 | | 0.4 | V |
| I/P current each I/O pin | I_i | $0.1V_{DD} < V_i < 0.9V_{DD}$ | -10 | | 10 | mA |

3.5.3. DC Characteristics: TX_FAULT; TX_DISABLE;LOS

| Parameter | | Comment | Min | Typ | Max | Unit |
|-------------------------|--|------------------------------|-------------------|-----|-------------------|------------|
| LVTTTL Voltage Out High | | External 4.7k to 10k pull-up | Host VCC - 0.5 | | Host VCC + 0.3 | V |
| LVTTTL Voltage Out Low | | External 4.7k to 10k pull-up | 0 | | 0.5 | V |
| LVTTTL Voltage In High | | Internal pull-up | 2.0 | | VDD + 0.3 | V |
| LVTTTL Voltage In Low | | Internal pull-up | 0 | | 0.8 | V |
| R pull-up | | Internal pull-up | 6 | | 10 | k Ω |

3.6. Typical Operating Characteristics

3.6.1. Electrical Receiver Eye Diagrams (3.3V; Ta = 25°C; PRBS 2⁷⁻¹)

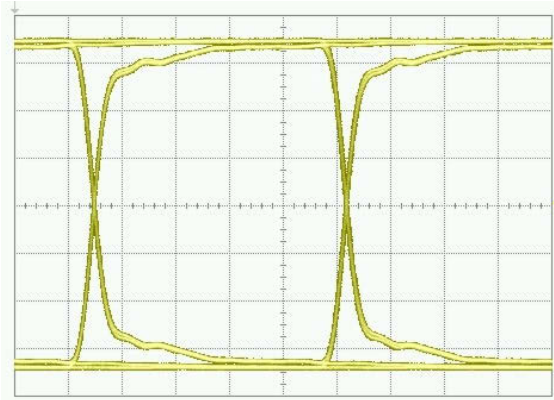


Figure 7 - 2.125Gbps High swing mode

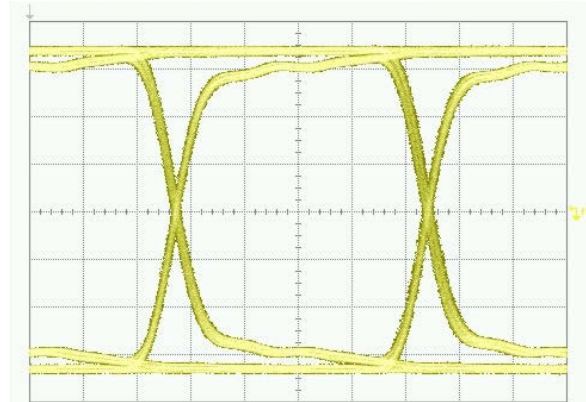


Figure 8 - 1.065Gbps High swing mode

3.6.2. Optical Transmit Eye Diagrams (3.3V; Ta = 25°C; PRBS 2²³⁻¹)

Transmitter setup with $P_{\text{mean}} = -3.5\text{dBm}$; E.R. = 10dB

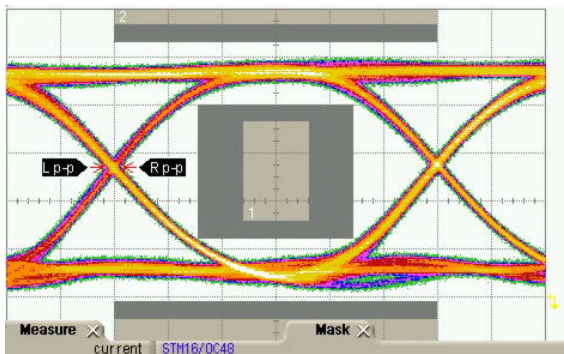


Figure 9 – 2.5 Gbps; STM16/OC48 Filter and mask

4. Functional Description

4.1. Overview

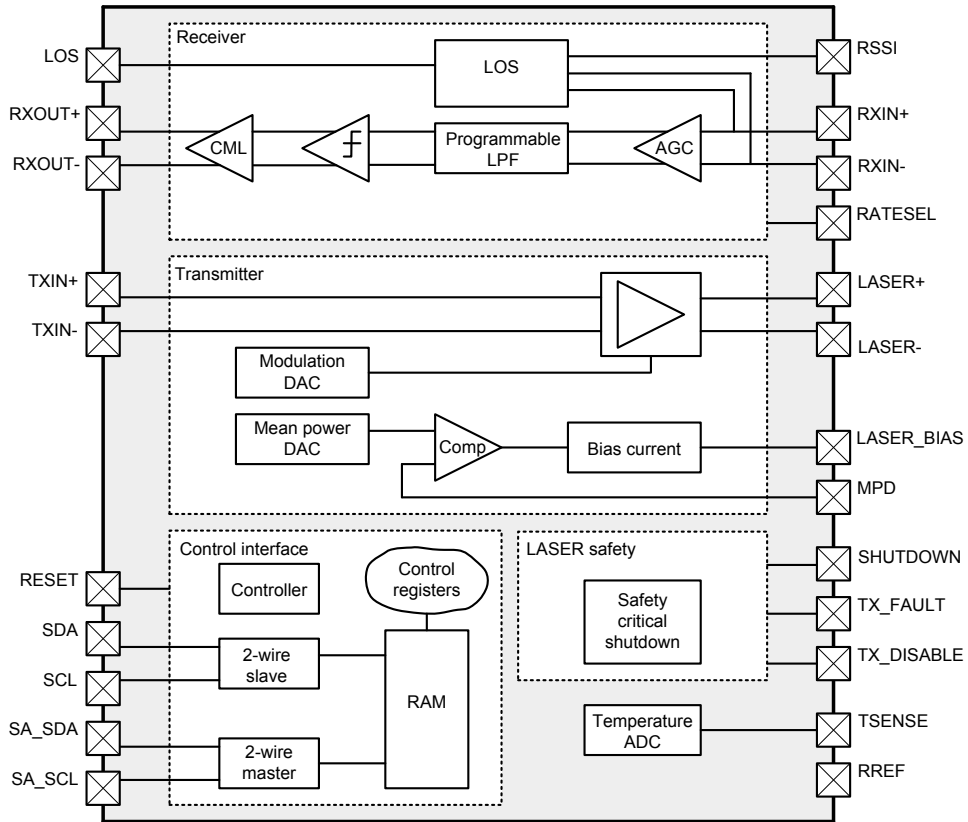


Figure 10 - Top-level block diagram of the PHY1076-01

4.2. Receiver Features

The receiver input is designed to be AC-coupled to the transimpedance amplifier, with internal 100Ω differential termination. The AGC amplifier is followed by a low-pass filter with programmable cut-off frequency, enabling the PHY1076-01 receiver to support six discrete data rates in the range 125 Mbps to 2.7 Gbps.

The filter output is followed by a limiting stage. For minimum duty cycle distortion, DC feedback from the limiter output is used for offset cancellation.

The output CML buffer completes the receiver chain, delivering the output at pins RXOUT+ and RXOUT-. The output edge rate is dependent on the programmable filter setting. Additionally, the output swing is programmable to satisfy different interface requirements (e.g. CML, AC-coupled LVPECL compatible).

The PHY1076-01 includes a regulator to deliver a controlled voltage to the receiver photodiode cathode at the RSSI pin. The current at RSSI is digitized for use in measuring the received signal strength. This signal can also be used to generate a Loss of Signal (LOS) alarm, with a pre-set hysteresis for assert and de-assert levels. The LOS assert threshold can be adjusted using the LOSS LEVEL DAC.

Alternatively, the LOS alarm can be programmed to detect the amplitude of the AC signal, the Optical Modulation Amplitude (OMA) at the receiver input. The OMA LOS assert threshold can be adjusted using the RX AMP DAC.

4.2.1. Input Stage Configuration

The differential RXIN inputs from the ROSA can be terminated to a common mode voltage. This should be used for all recommended application frequencies of the PHY1076-01, where the inputs are AC coupled. The common mode voltage should be connected by setting **RX_dccouple** = '0' (E8h **rxControl0** bit 3).

4.2.2. Rate Selection

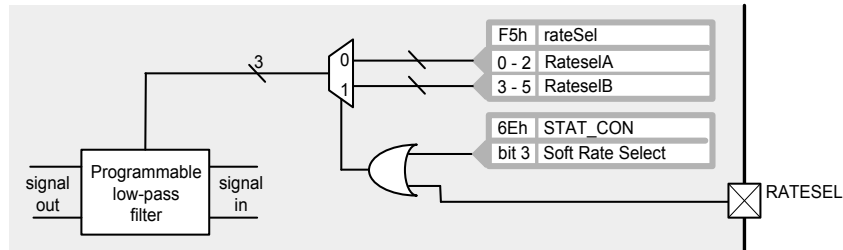


Figure 11 - Low pass filter rate selection

A programmable low pass filter provides band limiting in the received signal path. The filter bandwidth is set to 0.75 x signal data rate for optimum signal to noise performance and is controlled by a 3-bit control word as shown in Table 1.

The rate selection register, **rateSel**, stores two 3-bit codes for controlling the filter; code A in bits 0 to 2, and code B in bits 3 to 5. The selection between the two codes is determined by the RATESEL pin and the **Soft Rate Select** bit as shown in Figure 11. Thus, the RATESEL pin can be used to switch between two pre-selected rates.

The **rateSel** register is unique in that it is directly accessible from the 2-wire serial slave interface. Write accesses are routed to both the register in hardware and the RAM. Read accesses read the **rateSel** value from the hardware. This enables the PHY1076-01 to respond more quickly to updates of this register. This also means that during the initialization sequence, the bandwidth of the receiver can be set up before the **dsfail** alarm is cleared (see Section 5.2.2). This feature does not exist in the 2-wire serial master interface. When loading registers from EEPROM, **rateSel** is loaded via RAM in the same way as all other registers.

| Bit | | | Data Rate |
|-----|---|---|--------------|
| 2 | 1 | 0 | |
| 0 | 0 | 0 | 125/155 Mbps |
| 0 | 0 | 1 | 622 Mbps |
| 0 | 1 | 0 | 1062 Mbps |
| 0 | 1 | 1 | 1250 Mbps |
| 1 | 0 | 0 | 2125 Mbps |
| 1 | 0 | 1 | 2488 Mbps |
| 1 | 1 | 0 | No Filter |
| 1 | 1 | 1 | N/A |

Table 1 - Signal data rates supported by the low pass filter

4.2.3. CML Output Stage Configuration

The CML output stage has two slew rate settings. For maximum receiver eye opening set **CMLslew** = '0' (E8h **rxControl0** bit 0). To minimize emitted radiation set **CMLslew** = '1'. The slew rates are defined in the table of Parametric Performance characteristics for the Receive limiting amplifier (Section 3.3.1).

The signal swing can also be adjusted. Set **HiLoSwing** = '1' (E9h **rxControl1** bit 1) for higher amplitude differential output swing as defined in the table in section 3.3.1. Set **HiLoSwing** = '0' for lower amplitude output swing.

4.2.4. Loss Of Signal

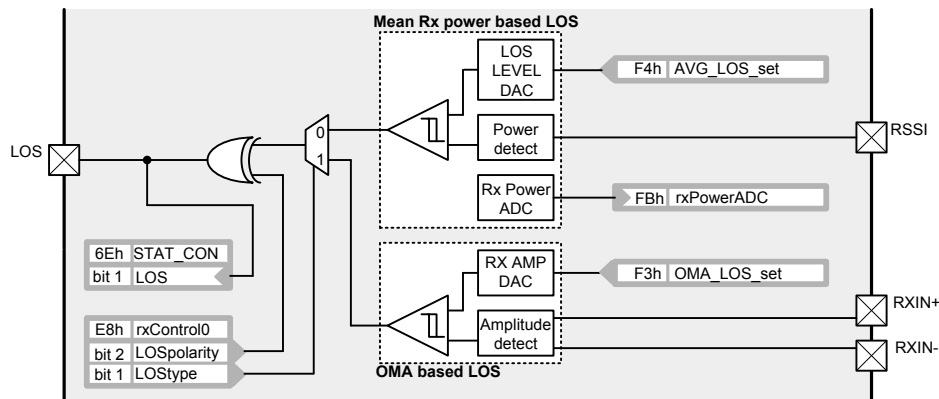


Figure 12 - Control of the LOS pin

Loss of signal (LOS) is determined in one of two ways. If **LOStype** = '1' then the optical modulation amplitude (OMA) method is selected. The signal amplitude measured at RXIN+/- is compared against a threshold level set by the **OMA_LOS_set** register. If the OMA does not exceed the threshold then the LOS pin and consequently the **LOS** bit in **STAT_CON** will be asserted.

If **LOStype** = '0' then the mean received power based method is selected. The signal power detected on the receiver signal strength indicator (RSSI) pin is compared against a threshold level set by **AVG_LOS_set**. If the RSSI does not exceed the threshold then the LOS pin and LOS bit are asserted.

The polarity of the LOS pin is controlled by **LOSpolarity**. If **LOSpolarity** = '0' then LOS is set high during a loss of signal condition. Conversely, if **LOSpolarity** = '1' then LOS is set high when a signal is detected.

| Register | DAC | Step Size | Threshold Range |
|-------------|---------------------------|--|--|
| AVG_LOS_set | LOS LEVEL DAC (8 bits) | For Codes 00h – 1Fh Step Size = $1.3\mu\text{A} \pm 0.4\mu\text{A}$ For Codes 1Fh – 7Eh Step Size = $4.6\mu\text{A} \pm 1.0\mu\text{A}$ | $0\mu\text{A}$ to $31\mu\text{A}$ $31\mu\text{A}$ to $411\mu\text{A}$ |
| OMA_LOS_set | RX AMP DAC (8 bits) | Use Codes 28h to C8h Step Size = $250\mu\text{V}$ (nominal DAC range = 0mV to 64mV) | 10mV to 50mV |

Table 2 - LOS DAC characteristics

For measurement of RSSI, which is used by SFF-8472 Digital Diagnostics Monitoring, the PHY1076-01 can be connected as shown in Figure 13, sourcing the photodiode bias current. This shows a PHY1093 TIA interfacing to the PHY1076-01. The photodiode used is biased using the regulated output of the PHY1076-01, providing a stable and low noise bias for the photodiode. The PHY1076-01 measures the photodiode current and generates a report of received signal strength via an on board A-D converter.

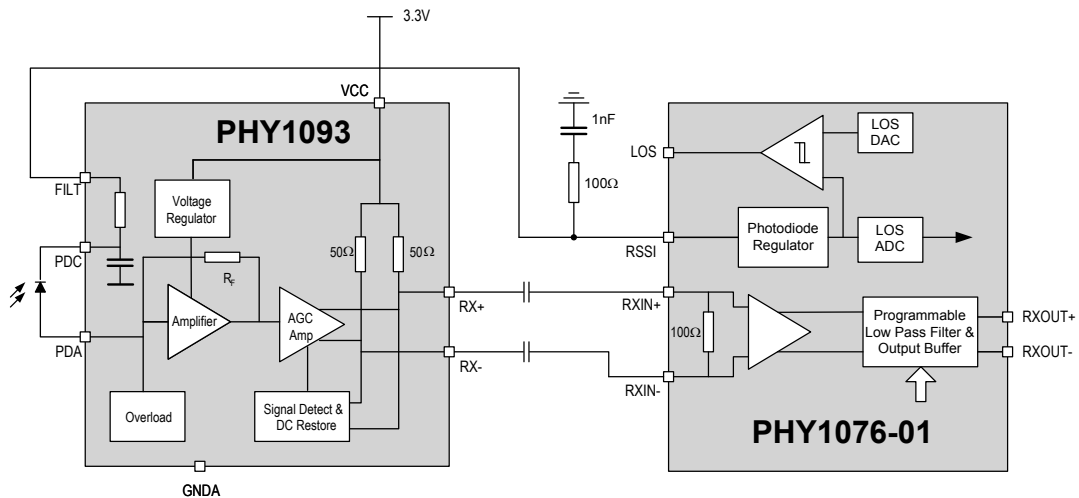


Figure 13 - Connection to TIA for RSSI method of LOS detection

In some cases the TIA may produce an output current which is proportional to the Received Signal Strength. In this case the application circuit shown in Figure 14 should be used. The current I_{RSSI} is mirrored using a dual NPN transistor as shown. This sinks an output current from the PHY1076-01 which can then be measured using the on chip ADC.

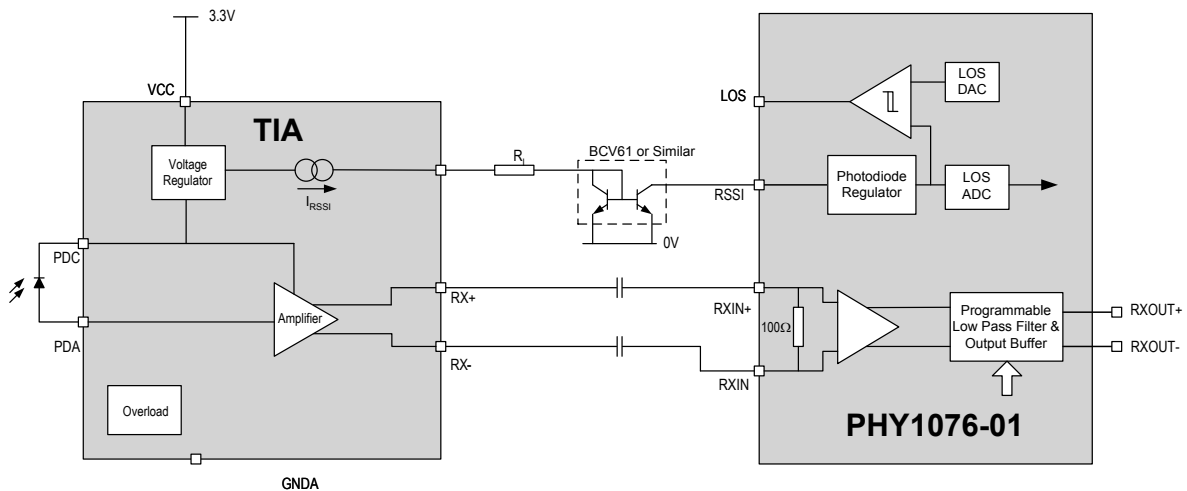


Figure 14 - Connection to TIA with integrated RSSI output

4.3. Transmitter Features

The transmitter input buffer provides the necessary drive to the Laser driver output stage. It is designed to be AC-coupled, with an internal 100Ω differential termination.

The Laser driver output is designed to drive Lasers in common-anode configuration, using either AC or DC coupling. The driver circuit delivers a maximum peak to peak modulation current of 70mA. The maximum current delivered in DC-coupled mode is dependent on the Laser impedance. The voltage swing must remain in the compliance range of the output stage as specified in section 3.4.2.

The PHY1076-01 Laser driver operates with an analog mean-power control loop, which is digitally programmed using the Mean Power DAC. Modulation current is controlled by a Laser modulation DAC with the characteristics shown in Table 3. The modulation DAC has a 375μA/bit resolution which suggests an upper limit of 96mA at full scale, however the modulation output stage is rated to 70mA only for jitter compliance. To satisfy the digital diagnostics requirements, the mean power, as represented by the monitor photocurrent, is measured using the MPD current monitor analogue to digital converter (Tx Power ADC). The bias current ADC (Tx Bias ADC) samples the Laser bias current.

| Register | DAC | Step Size | Rated Range |
|----------------------|---|---|-------------|
| tx_power_set | Mean Power DAC (8 bits) | 11μA±1.0μA (Actual DAC range 0μA to 3060μA) | 0 to 3mA |
| modulationDACDefault | Laser modulation DAC ¹ (8 bits) | 363μA±50μA (Actual DAC range is 0mA to 93mA) | 7mA to 70mA |

¹ Range of modulation current measured at LASER+/- (jitter within spec)

Table 3 - Characteristics of the modulation and bias current DACs

4.3.1. Bias Current Control

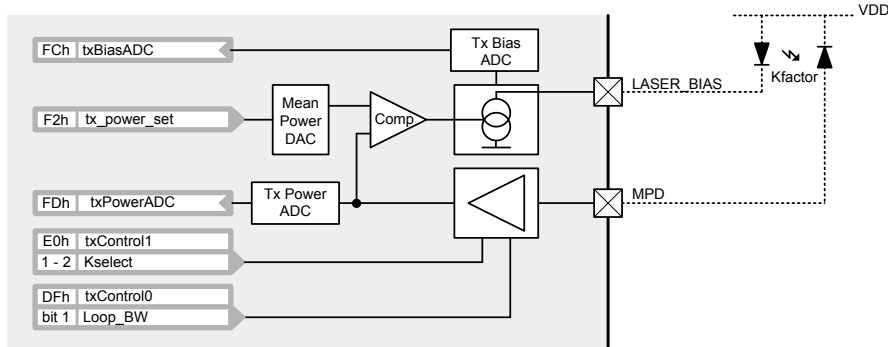


Figure 15 - Control registers affecting the APC loop

The Laser bias current is controlled by the mean-power control loop in which the current from the monitor photodiode in the TOSA is compared with a reference current controlled by **tx_power_set**. Note: the comparator is sensitive to large step changes in the value written to **tx_power_set** (or a small step change at low values). This can cause the safety critical shutdown module to assert a TX_FAULT, as will writing zero to **tx_power_set**.

Loop bandwidth and Kselect are used to optimize APC loop dynamics providing stability of the mean power control and the required transmitter start up time. These settings are affected by the coupling coefficient (Kfactor) between the Laser and monitor photodiode. The **Kselect** bits shown in Table 4 should be used as a guide for the set-up. For example, for a TOSA with Kfactor of 1/100 (Laser bias current = 50mA, monitor diode current = 0.5mA) set **Kselect** = "01".

Table 4 shows Kselect values that can be chosen to meet the start-up time and APC loop stability requirements:

| Coupling coefficient | Kselect value | |
|----------------------|---------------|---|
| | 1 | 0 |
| N/A | 0 | 0 |
| 1/500 – 1/50 | 0 | 1 |
| 1/50 – 1/25 | 1 | 0 |
| 1/25 – 1/8 | 1 | 1 |

Table 4 – Kselect guide for the APC loop

The bandwidth of the control loop response can be controlled with **Loop_BW**. For a critically damped loop, set **Loop_BW** to '0'. For a more rapid response, set **Loop_BW** to '1'. The frequency response of the loop is detailed in section 3.4.3 Laser Mean Power Control Loop.

4.3.2. Modulation Current Control

The modulation current can be controlled in two ways:

Set **ModLUTdisab** (DFh **txControl0** bit5) to '1' to directly access the modulation DAC. Then, adjust modulation current by writing to **modulationDACDefault** (D5h).

Set **ModLUTdisab** to '0' to enable the modulation current vs. temperature look-up table (LUT) in the PHY1076-01. The 45 byte LUT is indexed by the value in **temperatureADC** (FEh), where Index is given by:

$$\text{Index} = (\text{temperatureADC} \times 45) / 255$$

and the index rounds down to the lower temperature. When the LUT is switched from the enabled to disabled state, the last control value from the LUT will persist. On disabling the LUT the modulation DAC will not revert back to a value previously written to **modulationDACDefault**. A new value must be explicitly written to **modulationDACDefault** once the LUT has been disabled.

On power up the modulation DAC will not be programmed with the value uploaded from the EEPROM and will default to taking the value from the LUT for the measured temperature.

4.3.3. Laser Driver Setup

There is a trimming network on the output driver which adjusts the time constant for output damping on **LASER ±**. It is controlled by the value in **txDriverCap** (F6h) which is used to set the value of the time constant as shown in Table 5 based on the number of RC networks turned on. Set **txDriverCap** to '00' for no damping and fastest edges. It is possible to enable combinations by programming **txDriverCap** with values that set more than one bit high. e.g. **txDriverCap** = 07h enables **RxC/2 + RxC + Rx2C**.

| txDriverCap | Time constant (RC=34ps) |
|-------------|-------------------------|
| Bit 0 | RxC/2 |
| Bit 1 | RxC |
| Bit 2 | Rx2C |
| Bit 3 | Rx3C |
| Bit 4 | Rx4C |
| Bits 5 to 7 | Not used |

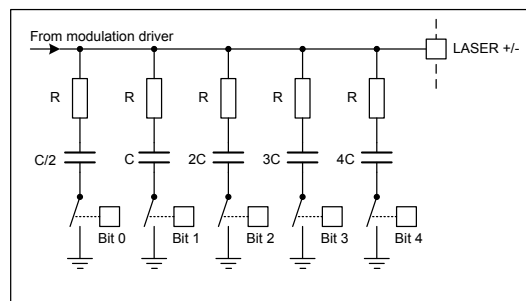


Table 5 -Time constant selection for the Tx output damping network.

4.4. Laser Safety Features

The Laser safety circuitry monitors the device for potential faults. If a fault is detected, the safety logic turns off the transmitter bias and modulation currents and indicates the fault condition at pin TX_FAULT.

The Laser output driver can be disabled in one of four ways:

1. The TX_DISABLE pin is taken high.
2. The internal safety critical shutdown circuitry detects a fault with
 - a. the APC loop or bias current
 - b. power supply $2.7V > VDD$ or $VDD > 3.9V$
 - c. RREF shorted to Ground, VDD or open circuit
3. The **Soft Tx Disable** bit in **STAT_CON** is asserted
4. The watchdog timer times out, indicating that communication with the host/MCU has been interrupted.

In all cases the modulation current and the current to the LASER_BIAS pin will be disabled, and the SHUTDOWN pin will be asserted. The purpose of the SHUTDOWN pin is to provide a means by which the Laser can be isolated from VDD (common anode configuration) when an electrical fault is detected. In cases 2 and 4, TX_FAULT will also be set.

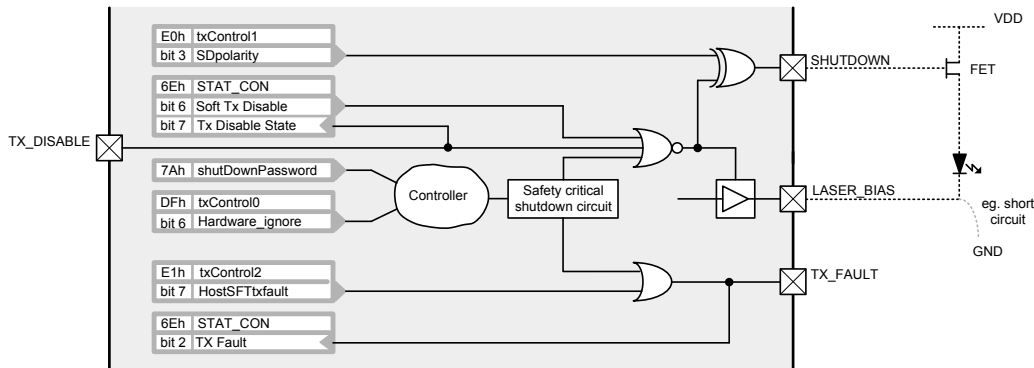


Figure 16 - TX_FAULT and SHUTDOWN pin control logic

4.4.1. PHY1076-01 Fault Management

The safety critical shutdown circuit will shutdown and isolate the Laser if it senses a fault with the bias current, the supply voltage or the reference voltage.

For example, consider a Laser arranged in common anode configuration. The Laser cathode connects to the LASER_BIAS pin and the anode connects to VDD. If a short circuit to Ground occurs on the route between the cathode and LASER_BIAS then the safety critical shutdown circuit will switch off the bias current. However, this will not protect the Laser as a current path from VDD to ground still exists. A FET device can provide the required isolation when switched off by the SHUTDOWN pin as shown in Figure 16. The SHUTDOWN pin is controlled by the same signal which switches off the bias current. The SHUTDOWN pin output response to faults and polarity setting is shown in Table 6.

The safety critical shutdown circuit can be disabled in software by setting **Hardware_ignore** = '1', and entering the value 42h to the **shutDownPassword** register. In this case the Laser will not be disabled when a fault is detected; however, a TX_FAULT will still be reported. **This feature should be used with great caution as the eye safety features of the device will be disabled.** The PHY1076-01 will respond to TX_DISABLE being set even if **Hardware_ignore** is set.

Power supply and RREF faults result in the TX_FAULT latching and the laser being disabled momentarily. Once the fault condition is removed the laser will be reactivated, however the TX_FAULT output must be cleared by toggling TX_DISABLE (or **Soft Tx Disable**). An APC loop fault results in the TX_FAULT latching and the laser being disabled. TX_DISABLE (or **Soft Tx Disable**) must be pulsed high as shown in Figure 5 to remove this latching condition and reactivate the laser. When the Laser is turned on, during

power up or after a fault, there will be a short period during which the bias control loop is allowed to settle (t_{settle} , see Section 3.4.3) before the safety control loop circuit is enabled.

| Fault Status | SDpolarity (TxControl2, Bit 3) | SHUTDOWN Pin Voltage |
|---------------------|---|---------------------------------|
| No Fault | 0 | High |
| | 1 | Low |
| Fault | 0 | Low |
| | 1 | High |

Table 6 – Shutdown Output Voltage under Fault/No Fault conditions

4.4.2. MCU and Host Fault Management

The MCU is responsible for maintaining and reporting alarms and warnings in accordance with the SFF-8472 specification. When an alarm is triggered, the MCU must set **HostSFTtxfault** = '1'. This will cause the PHY1076-01 to report a fault on the TX_FAULT pin and in the **STAT_CON** register. The PHY1076-01 will not disable the Laser at this point. The MCU or the host could disable the Laser when a **TX Fault** is detected in **STAT_CON** by asserting **Soft Tx Disable**.

4.4.3. Watchdog

A watchdog is implemented by the PHY1076-01 to monitor the activity of the attached MCU in digital diagnostics mode. When **WatchdogEn** (E1h **txControl2** bit0) is set to '1', the PHY1076-01's watchdog feature is enabled. The MCU is required to increment the **Watchdog[0:5]** counter (E1h **txControl2**) at least every 100ms. If no change is detected in the counter, the PHY1076-01 will disable the Laser and will assert TX_FAULT. The Laser will be re-enabled, and TX_FAULT de-asserted when either the watchdog counter is incremented, or the watchdog feature is disabled by writing '0' to **WatchdogEn**. On power up the watchdog feature is disabled.

4.5. Tsense Temperature Sensor

The temperature is determined by measuring the ΔV_{BE} across an external transistor connected to the TSENSE pin. The transistor can be any standard npn silicon transistor with a beta > 100 connected in diode mode (base and collector tied together). It is recommended to use a BC847B or similar.

Calibration and averaging of the temperature sensor readings using an external microcontroller are required to optimize the accuracy. Once optimized, the PHY1076-01 can report temperature to SFF8472 requirements over the recommended operating conditions.

The temperature sensor operating range and corresponding TSENSE input levels are shown in Table 7.

| | Symbol | Unit | Minimum | Maximum |
|----------------------------|-----------------|------|---------|---------|
| Temperature | t | °C | -70 | +115 |
| TSENSE delta input voltage | ΔV_{BE} | mV | 50 | 100 |

Table 7 – Temperature sensor operating range

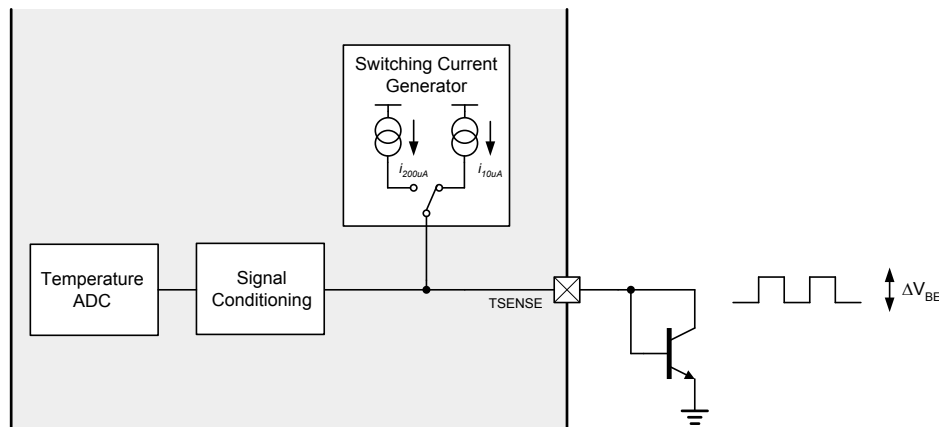


Figure 17 – Temperature sensor functional block diagram

5. Control Interface

The PHY1076-01 can be operated in one of two modes as dictated by the design of the module. The PHY1076-01 will identify the mode by attempting to read from its 2-wire serial EEPROM interface (See section 5.4) on power up. If no EEPROM is present then diagnostic mode is inferred.

In digital diagnostics mode, the Micro Controller Unit (MCU) and EEPROM (Address A0h) present an SFF-8472 compliant interface to the host. The MCU provides read/write access to all registers in the A2h registers map, calculates digital diagnostics monitor values and maintains alarms and warnings. The MCU must initialize the PHY1076-01 control registers from EEPROM, relay control information to the PHY1076-01, and fetch status information in real time.

In stand-alone mode, the PHY1076-01 is initialized directly from an external 4 kbit (8 x 512 bit) Serial EEPROM. Serial ID information as specified in the SFP MSA is accessible via the 2-wire serial interface. This mode supports temperature compensation of modulation current using a look-up table stored in EEPROM.

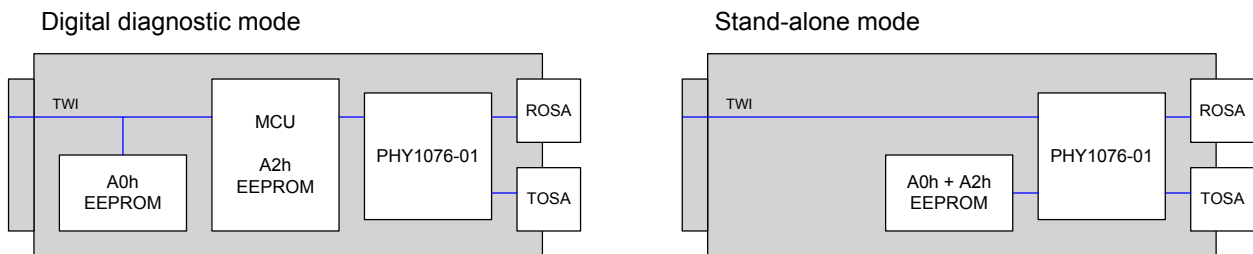


Figure 18 - Optical transceiver module configurations

5.1. Memory Map

| A0h | A2h tabel = 00h or 01h | A2h tabel = 02h | A2h tabel = 03h | |
|---|--|---|---|-----|
| SFF-8472 Serial ID Serial ID (96) Vendor specific (32) | SFF-8472 Diagnostics SFP MSA Diag (120) Vendor specific (7) | PHY1076-01 Expansion EEPROM Undefined (127) | PHY1076-01 Expansion EEPROM Undefined (127) | 7Fh |
| | | | | |
| SFF-8472 Reserved (128) | SFF-8472 U. EEPROM User EEPROM (120) Vendor specific (8) | PHY1076-01 Expansion EEPROM Undefined (128) | Device Settings (128) | |

Figure 19 - Memory map for a 2G SFP or SFF transceiver module containing a PHY1076-01 device

Figure 19 shows the memory map of a module containing a PHY1076-01. An 8 kbit memory space is a natural step up from the minimum 4 kbit memory space required for SFF-8472 compliance, providing additional space in which to map the Device Settings registers of the PHY1076-01.

The internal RAM of the PHY1076-01 implements the SFF-8472 Diagnostics table and the Device Settings table. Selection between tables is achieved using the **tableSelect** (tabel) register located at address offset 7Fh. To access the Diagnostics table, first write 00h to tabel. To access the Device Settings table, first write 03h to tabel.

Tabel is effectively write-only because to write to tabel has the effect of switching to a different register table. Thus, reading tabel will not yield the value which was previously written.

5.2. Operation

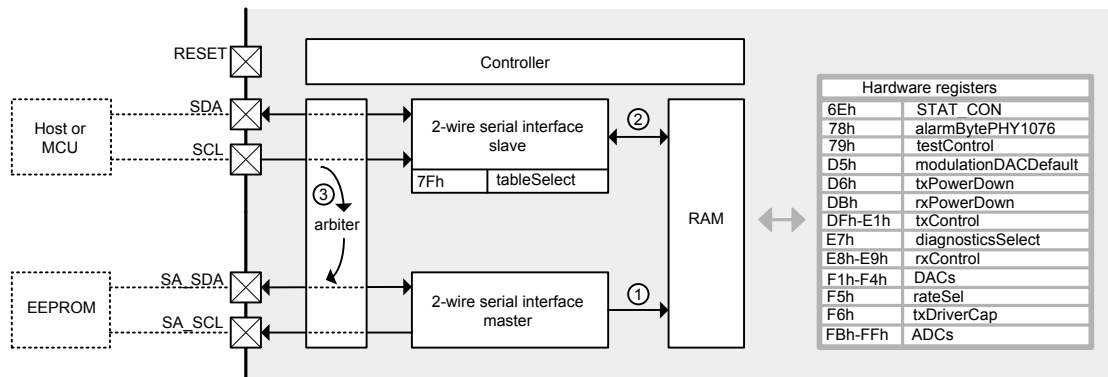


Figure 20 - Serial interfaces to RAM and the on-chip controller

5.2.1. Data Transfer Mechanisms

Three distinct data paths are identified in Figure 20.

When the PHY1076-01 comes out of reset, the 2-wire serial slave interface is disabled. Only path 1 is active. The controller instructs the 2-wire serial master interface to attempt to transfer A2h register tables (SFF-8472 diagnostics and device settings) from the external EEPROM to RAM. If this is successful then the PHY1076-01 will operate in stand-alone mode. If the transfer fails, then the **dsfail** and **eerxfail** alarm bits in the **alarmBytePHY1076** (78h) register will be set and the PHY1076-01 will operate in diagnostics mode. Regardless of the outcome, when the EEPROM read process is complete the controller enables the 2-wire serial slave interface. The 2-wire serial master interface is then no longer used.

The 2-wire serial slave interface has slave address A2h. In diagnostics mode, the host or external MCU uses the 2-wire serial slave interface to write to or read from copies of the device settings held in RAM. When the boot sequence is complete, the controller transfers data between the RAM and the actual registers implemented in hardware periodically every 10ms.

In stand-alone mode the RAM space is not used once the boot sequence is complete. Reading from A2h will return zero.

Path 3 is a special case which supports modules designed for stand-alone mode, enabling them to be set up or re-configured via the 2-wire serial interface slave. The PHY1076-01 can be forced into diagnostic mode if the data integrity numbers in the EEPROM are deliberately erased (see section 5.4.2). This enables the host/MCU to access both the RAM (path 2) and the EEPROM (path 3). All accesses to the A0h address space are directed to the EEPROM only. Accesses to the A2h address space are examined as they arrive by the 2-wire serial slave module, which in turn instructs the arbitration logic. The destination for the transaction depends on the value of **tableSelect** and the register address as shown in Table 8.

| Access type | tabssel | Address range ¹ | Destination memory |
|-------------|---------|----------------------------|--------------------|
| read | 00 | lower | RAM |
| read | 03 | upper | RAM |
| write | 00 | lower | RAM + EEPROM |
| write | 00 | upper | EEPROM |
| write | 03 | upper | RAM |

1 Addresses 00h to 7Fh = lower. Addresses 80h to FFh = upper.

Table 8 - Destination of 2-wire serial interface transactions as a function of write protection, tabssel and address.

5.2.2. Device Initialisation Sequence

The Initialisation Sequence is illustrated in Figure 21. The **Data_Ready_Bar** bit in the **STAT_CON** register indicates when data from the ADCs may be read after power up. It is first set to '1' before the 2-wire serial slave interface is enabled to indicate that the PHY1076-01 is not ready. Once initialisation is complete and the ADC data is ready **Data_Ready_Bar** is cleared to '0'. This event can be used by the external host/MCU as a signal that the PHY1076-01 is ready for device settings to be uploaded from the MCU to the PHY1076-01 RAM. The PHY1076-01 will not enter the main diagnostic function loop until the upload is complete. This is initiated by the host/MCU clearing the **dsfail** and **eerxfail** bits in the **alarmBytePHY1076** (78h) register. When **dsfail** is cleared and the main loop is executed the contents of RAM will be transferred into the hardware registers of the PHY1076-01.

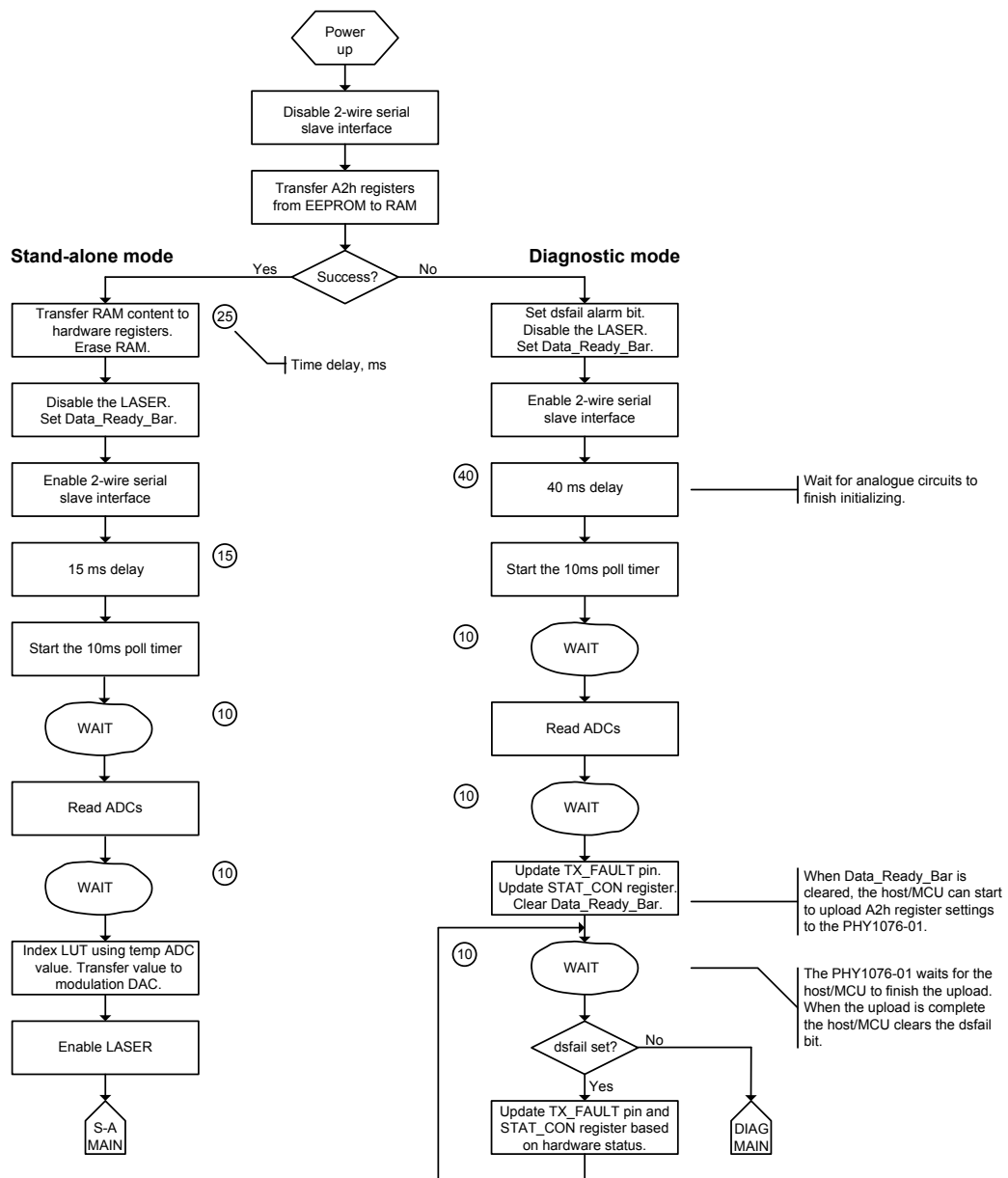


Figure 21 - PHY1076-01 initialisation sequence. Time delays for key stages are shown in ms.

5.2.3. Polling Loop Timer

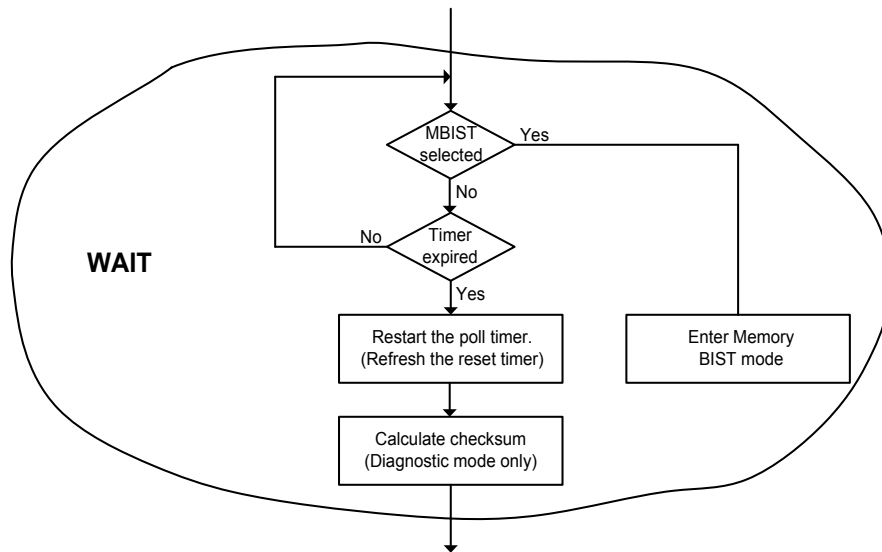


Figure 22 - PHY1076-01 polling loop timer function.

A polling loop timer is implemented in the controller which expires every 10ms. This is used to schedule functions in both the boot sequence and the main diagnostic and stand-alone operating modes. The WAIT clouds shown in the flow diagrams represent the sequence of events shown in Figure 22.

The reset timer is the timer enabled by **wdlInhibit** in the **diagnosticsSelect** register (E7h). Refer to the registers map for details.

The checksum function is executed in diagnostic mode only. The PHY1076-01 will generate a checksum of the device settings RAM area by addition of each of the bytes listed in Table 9, and store the result in the 16 bit **ddmChecksum** register (E5h to E6h) in big endian format. The checksum will allow the MCU to efficiently verify that the copies of these registers in the PHY1076-01 and in its own memory are coherent.

| Address | Size (bytes) | Name |
|---------|--------------|--------------|
| 80h | 40 | Reserved |
| A8h | 45 | currentLUT |
| D6h | 1 | txPowerDown |
| D7h | 4 | undefined |
| DBh | 1 | rxPowerDown |
| DCh | 3 | undefined |
| E8h | 2 | rxControl |
| F1h | 1 | Vref |
| F2h | 1 | tx_power_set |
| F3h | 1 | OMA_LOS_set |
| F4h | 1 | AVG_LOS_set |
| F5h | 1 | rateSel |

Table 9 - Registers included in the checksum calculation

5.2.4. Controller Main Application Loop Functions

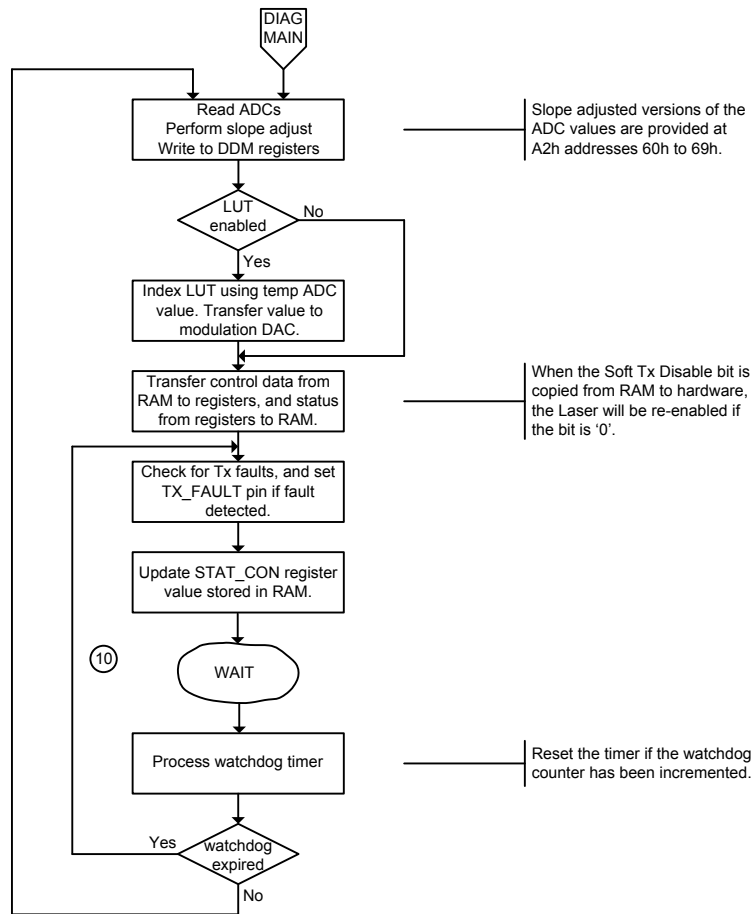


Figure 23 - PHY1076-01 diagnostic mode main loop function.

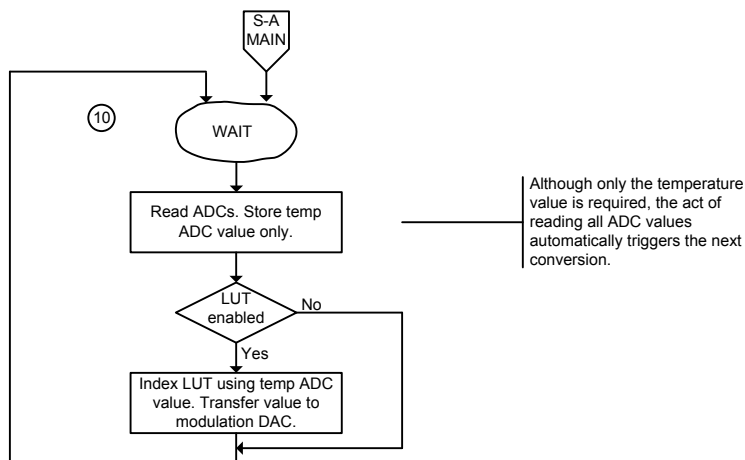


Figure 24 - PHY1076-01 stand-alone mode main loop function.

5.3. Digital Diagnostics Mode

5.3.1. Introduction

When used in digital diagnostic mode the PHY1076-01 contains all of the necessary analogue and digital circuitry to generate the real time values required for SFF-8472 DDM reporting compliance. The power supply voltage, Temperature, TxBias, MPD and RSSI are all sampled using an on board A/D converter. The digitized values are then made available over the slave 2-wire serial interface, such that they can be used in conjunction with SFF-8472 calibration constants, to provide the host user with the following five real time reports: Supply Voltage, Temperature, Tx Bias current, Tx Output Power and Rx Input Power.

5.3.2. On Chip Analogue to Digital Converter

The PHY1076-01 contains a single successive approximation ADC. The ADC coding is either linear or multi-slope, depending on the parameter being sampled. The multi-slope stage enables the ADC to cover the very large dynamic range required for reporting Tx and Rx optical power within the SFF-8472 limits, using only 8-bits to cover an equivalent 12-bit dynamic range. The ADC conversion time takes approximately 1ms.

5.3.3. ADC Characteristics

| DDM Name | ADC input | Nominal Range | Step Size | Slope Accuracy | Accuracy |
|----------------|-------------|---------------------|-----------|----------------|-------------|
| Supply Voltage | VDD | Min 1.6 – 1.9V | 11 mV | ±1.5mV | |
| | | Max 4.1 – 5.0V | | | |
| Temperature | Temperature | -70°C to +115°C | 0.83 °C | | |
| Tx Bias | TxBias | 0.0mA to 100mA | 0.5mA | | |
| Tx Power | MPD | 0.0µA to 32.0µA | 0.96µA | ±0.2µA | ±3µA Offset |
| | | 32.0µA to 416.0µA | 4.2µA | ±0.4µA | |
| | | 416.0µA to 2448.0µA | 16 µA | ±1.5µA | |
| Rx Power | RSSI | 0.0µA to 32.0µA | 1.07µA | ±0.2µA | ±3µA Offset |
| | | 32.0µA to 416.0µA | 4.3µA | ±0.4µA | |
| | | 416.0µA to 2448.0µA | 17.3µA | ±1.5µA | |

Table 10 – ADC electrical characteristics

5.3.4. 3-Slope ADC

Tx and Rx Power DDM reports are represented by an 8 bit (0-255) ADC value even though the overall dynamic range for both of these parameters is 0µA to 2448 µA. A linear coding scheme would only provide 9.5µA resolution at low currents. Acceptable low current resolution coupled with wide dynamic range is possible by using a multi-slope gain stage within the ADC circuitry. The following formulae are used to convert the 8-bit ADC (0 to 255) value into a linear pseudo 12-bit ADC (0 to 2448) value:

$$\begin{aligned}
 0 < \text{ADC} \leq 32: & \quad \text{ADC_L} = \text{ADC} \\
 32 \leq \text{ADC} \leq 128 & \quad \text{ADC_L} = ((\text{ADC} - 32) * 4) + 32 \\
 128 \leq \text{ADC} \leq 255 & \quad \text{ADC_L} = ((\text{ADC} - 128) * 16) + 416
 \end{aligned}$$

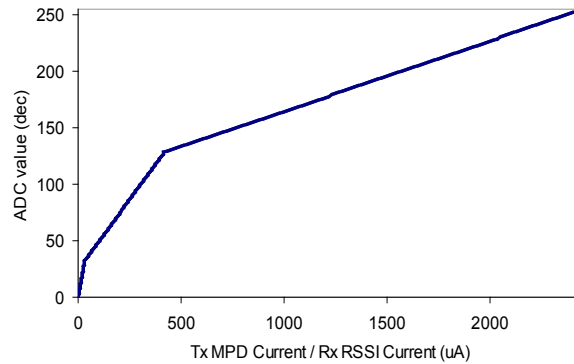


Figure 25– 3-slope ADC Function

5.3.5. ADC DDM Register Locations

The 8-bit ADC values can be accessed in their raw format at addresses FBh to FFh (tabel = 03h). The ADC values are also accessible at addresses 60h to 69h (tabel = 00h) where Tx Power and Rx Power ADC values are linearized by the PHY1076-01 and, therefore, do not require any conversion from 3-slope format unlike the raw 8-bit ADC values.

An external MCU is required to apply the correct calibration *slope* and *offset* values to the PHY1076-01 ADC DDM reports in order that the real time reports are meaningful. Table 11 shows the memory locations that should be addressed on the 2-wire slave interface to access the various DDM ADC values. All 8 bit or 12 bit ADC values are left aligned into the 16 bit registers with unused bits set to zero. For example the MSBit of Tx Output Power is located at the MSBit of 66h (tabel = 00h).

| Address | Location | Name | Size |
|------------------------------|------------|----------------|--------|
| Table Select Byte (7F) = 00h | | | |
| A2h | 60h to 61h | Temperature | 16-bit |
| A2h | 62h to 63h | Vcc | 16-bit |
| A2h | 64h to 65h | Tx Bias | 16-bit |
| A2h | 66h to 67h | Tx Power | 16-bit |
| A2h | 68h to 69h | Rx Power | 16-bit |
| Table Select Byte (7F) = 03h | | | |
| A2h | FBh | rxPowerADC | 8-bit |
| A2h | FCh | txBiasADC | 8-bit |
| A2h | FDh | txPowerADC | 8-bit |
| A2h | FEh | temperatureADC | 8-bit |
| A2h | FFh | vddADC | 8-bit |

Table 11 – ADC DDM register locations

5.4. Stand-Alone Mode

In stand-alone mode, the PHY1076-01 is initialized directly from an external 4 kbit (8 x 512 bit) Serial EEPROM. In normal operation, there is no access to the device settings information via the 2-wire serial interface. However, the Serial ID information as specified in the SFP MSA is still accessible. This mode supports temperature compensation of modulation current using a look-up table stored in EEPROM.

5.4.1. Data Integrity Checking

The (read-only) ADCs located at addresses FBh to FFh are dual-functioned with (write-only) data integrity registers as follows:

| Addr | Register | Value(hex) |
|------|-------------------------|------------|
| FBh | SerialEepromIdentifier0 | 1Bh |
| FCh | SerialEepromIdentifier1 | 2Ch |
| FDh | SerialEepromIdentifier2 | 3Dh or 4Eh |
| FEh | SerialEepromChecksum0 | -- |
| FFh | SerialEepromChecksum1 | -- |

Table 12 - Mapping of the data integrity numbers

On power-up, the PHY1076-01 will attempt to load its RAM from the EEPROM. If this is unsuccessful then **eerxfail** and **dsfail** are both set to '1' (78h **alarmBytePHY1076**) and initialisation will be stalled. If the transfer is successful then the integrity of the data will be checked. This process is carried out in the following sequence of events.

First the PHY1076-01 checks that the data read from EEPROM at addresses FBh to FCh matches the values shown in Table 12. If there is a mismatch then **dsfail** is set to '1' and initialisation will be stalled.

If **SerialEepromIdentifier2** = 3Dh then the PHY1076-01 will accumulate a 16 bit checksum for the A2h RAM address range 00h to FAh (excluding 7Fh). If this accumulated checksum does not compare correctly with the two **SerialEepromChecksum** bytes, then **dsfail** will be set to '1' and initialisation will be stalled.

Once all checks are complete, if no alarms have been set then the hardware registers in the PHY1076-01 are updated from the RAM. Data in RAM addresses FBh to FFh will subsequently be overwritten by the ADCs.

5.4.2. Device Setup

If a module is powered up with a blank or corrupted EEPROM then the data integrity checking will fail and initialisation is stalled. However, the PHY1076-01 can be forced into a 'setup' mode if the **dsfail** alarm is cleared by the host. This then permits the device to be configured and the EEPROM written in-system.

To reconfigure or analyse a module with its EEPROM already written, writing zero to the data integrity register addresses in EEPROM will have the effect of forcing the PHY1076-01 into setup mode the next time it is powered up.

5.4.3. Writing to EEPROM

The addressing of the RAM in the PHY1076-01 is consistent with the memory map for the module as a whole (see Figure 19). The table containing the SFF-8472 Diagnostics registers is selected by **tabsel** = 0 and the table containing the Device settings registers is selected by **tabsel** = 3.

The serial EEPROM connected to a PHY1076-01 in stand-alone mode is typically small and is organized as shown below:

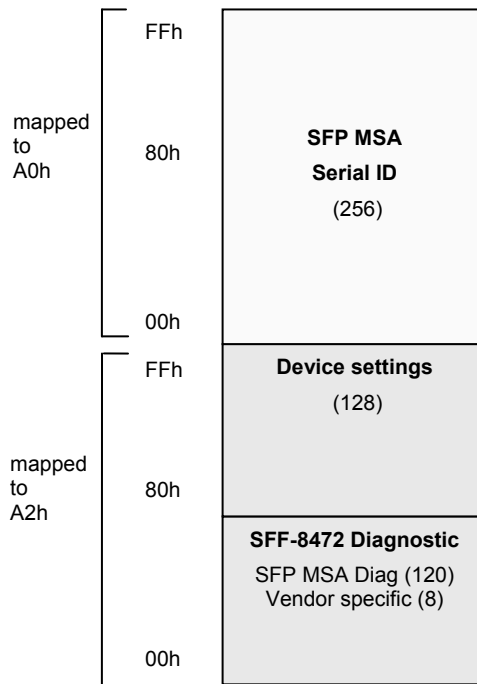


Figure 26 - Physical mapping of register tables into the EEPROM in the stand-alone mode

The device settings area in EEPROM is effectively stored in the address range normally occupied by the SFF-8472 User EEPROM (in Diagnostics mode). When writing to Device settings two separate write transactions are required: one write (into RAM) with tabsel = 3, and one write (into EEPROM) with tabsel = 0. It is recommended that the write protect functionality of the EEPROM is utilized to effectively protect stored settings after programming.

5.5. 2-wire Serial Interface

The PHY1076-01 has a pair of 2-wire serial interfaces - a slave for interfacing to an external MCU for use in diagnostics mode and a master for interfacing to an external EEPROM for use in stand-alone mode. Both interfaces communicate using the protocol described in this section.

5.5.1. Framing and Data Transfer

The 2-wire interface comprises a clock line (SCL) and a data line (SDA). When the bus is idle both are pulled high within the PHY1076-01 by 8 k Ω pullups.

An individual transaction is framed by a start condition and a stop condition. A start condition occurs when a bus master pulls SDA low while the clock is high. A stop condition occurs when the bus master allows SDA to transition low-to-high when the clock is high. Within the frame, the master has exclusive control of the bus. The PHY1076-01 does not support REPEAT START conditions whereby the master may simultaneously end one frame and start another without releasing the bus by replacing the STOP condition with a START condition.

Within a frame, the state of SDA may only change when SCL is low. A data bit is transferred on a low-to-high transition of SCL. Data is arranged in packets of 9 bits. The first 8 bits represent data to be transferred (most significant bit first). The last bit is an acknowledge bit. The recipient of the data holds SDA low during the ninth clock cycle of a data packet to acknowledge (ACK) the byte. Leaving SDA to float high on the ninth bit signals a not-acknowledged (NACK) condition. The interpretation of the acknowledge bit by the sender will depend on the type of transaction and the nature of the byte being received.

5.5.2. Device Addressing

The first byte to be sent after a START condition is an address byte. The first seven bits of the byte contain the target slave address (msb first). The eighth bit indicates the transaction type – ‘0’ = write, ‘1’ = read. Each slave interface on the bus is assigned a 7-bit slave address. If no slave matches the address broadcast by the master then SDA will be left to float high during the acknowledge bit and the master receives a NACK. The master must then assert a STOP condition. If a slave identifies the address then it acknowledges the master and proceeds with the transaction identified by the type bit.

The slave interface of the PHY1076-01 can decode slave addresses A0h and A2h.

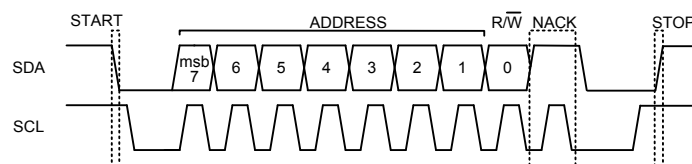


Figure 27 - Address decoding example – slave not available

5.5.3. Write Transaction

Figure 28 shows an example of a write transaction. The address byte is successfully acknowledged by the slave, and the type bit is set low to signify a write transaction. After the acknowledge the master sends a single data byte. All signalling is controlled by the master except for the SDA line during the acknowledge bits. During the acknowledge the direction of the SDA line is reversed and the slave pulls SDA low to return a ‘0’ (ACK) to the master.

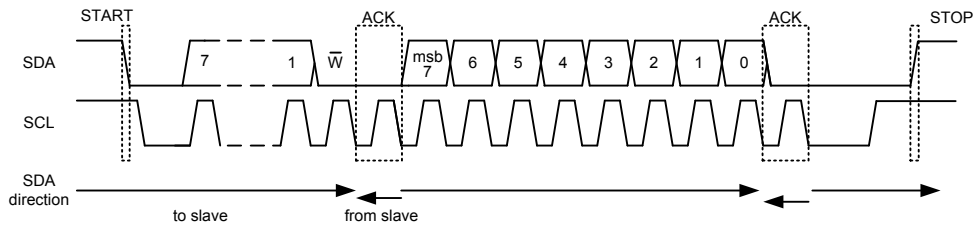


Figure 28 - Write transaction

If the slave is unable to receive data then it should return a NACK after the data byte. This will cause the master to issue a STOP and thus terminate the transaction.

The PHY1076-01 interprets the first data byte as a register address. This will be used to set an internal memory pointer. Subsequent data bytes within the same transaction will then be written to the memory location addressed by the pointer. The pointer is auto-incremented after each byte. There is no limit to the number of bytes which may be written in a single burst to the 256 byte internal RAM of the PHY1076-01.

If the slave is not ready to receive a byte then it may hold SCL low immediately after the acknowledge bit. When SCL is released the master starts to send the next byte. This is known as clock stretching. The PHY1076-01 slave interface will not clock stretch at up to 100 kHz SCL frequency.

5.5.4. Read Transaction

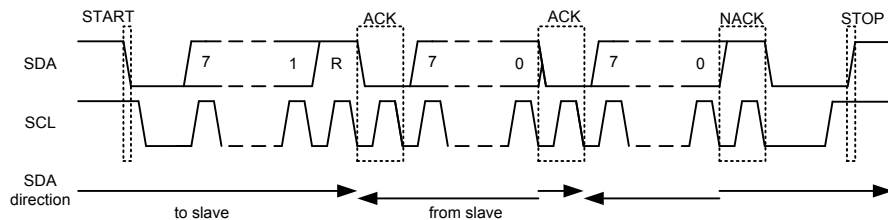


Figure 29 - Read transaction

Figure 29 shows an example of a 2 byte read transaction. The address byte is successfully acknowledged by the slave, and the type bit is set high to signify a read. After the ACK the slave returns a byte from the location identified by the internal memory pointer. This pointer is then auto-incremented. The slave then releases SDA so that the master can ACK the byte. If the slave receives an ACK then it will send another byte. The master identifies the last byte by sending a NACK to the slave. The master then issues a STOP to terminate the transaction.

Thus, to implement a random access read transaction, a write must first be issued by the master containing a slave address byte and a single data byte (the register address) as shown in Figure 28. This sets up the memory pointer. A read is then sent to retrieve data from this address (see Figure 29).

6. Register Map

All Maxim Integrated-specific registers are listed in this section. For details of other registers refer to the SFF-8472 Specification for Diagnostic Monitoring Interface for Optical Transceivers.

Where a single power-on reset (PoR) value is shown for a range of addresses, that value applies to all bytes in the range. Note that the power on reset values may be overwritten during initialisation by the MCU (or from EEPROM in stand-alone mode).

For registers containing a single 8-bit field, the most significant bit of the field is stored in bit 7 of the register byte. Multi-byte registers are stored in big-endian order unless specified otherwise.

Note that 'reserved' or 'internal use only' register bits are specified as read only. These registers should not change from their PoR default settings.

| 6Eh | STAT_CON | | | Status and Control register for some SFF-8472 functions |
|-----|----------------------|------|-----|--|
| Bit | Field name | Type | PoR | |
| 7 | Tx Disable State | R | 0 | Digital state of the TX Disable input pin. Updated within 100msec of change of pin. |
| 6 | Soft TX Disable | R/W | 0 | Read/write bit that allows software disable of laser. Writing '1' disables laser. This bit is "OR'd" with the hard TX_DISABLE pin value. |
| 5 | Reserved | R | 0 | Reserved for future use. |
| 4 | Rx Rate Select State | R | 0 | Digital state of the SFP RX Rate Select input pin. Updated within 100msec of change on pin. |
| 3 | Soft RX Rate Select | R/W | 0 | Soft RX Rate Select read/write bit that allows software RX rate select. Writing '1' selects full bandwidth operation. This bit is "OR'd" with the RATE_SELECT pin value. |
| 2 | TX Fault | R | 0 | Digital state of the TX_FAULT output pin. Updated within 100msec of change on the pin. |
| 1 | LOS | R/W | 0 | Digital state of the LOS output pin. Updated within 100msec of change on the pin. |
| 0 | Data_Ready_Bar | R | 0 | Indicates PHY1076-01 has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low. |

| | | | | |
|------------|-------------------------|-------------|------------|---|
| 78h | alarmBytePHY1076 | | | Status register for the PHY1076-01 control module. |
| Bit | Field name | Type | PoR | |
| 7 | Wd4 | R | 0 | This counter records the number of times that the PHY1076-01 has reset itself due to an internal timeout. The timer is controlled by wdlInhibit in the diagnosticsSelect register. |
| 6 | Wd3 | R | 0 | |
| 5 | Wd2 | R | 0 | |
| 4 | Wd1 | R | 0 | |
| 3 | Wd0 | R | 0 | |
| 2 | membistPassed | R | 0 | Built-in self test (BIST) result ('1' = passed) from memory test initiated by testControl register bit 1. |
| 1 | dsfail | R/W | 0 | Data structure corrupt ('1' = data integrity bytes read from EEPROM during power up are incorrect). Clearing this bit during initialisation is necessary in order to allow the PHY1076-01 to resume its normal mission mode functions. |
| 0 | eerxfail | R | 0 | EEPROM dma load fail. ('1' = no response from EEPROM during power up) |

| | | | | |
|------------|--------------------|-------------|------------|---|
| 79h | testControl | | | This register puts the device into various test modes and should not be written to during normal operation. It should always have value '0'. |
| Bit | Field name | Type | PoR | |
| 7 | ATBcontrol5 | R/W | 0 | Analog Test Bus Control Bit0 |
| 6 | ATBcontrol4 | R/W | 0 | Analog Test Bus Control Bit1 |
| 5 | ATBcontrol3 | R/W | 0 | Analog Test Bus Control Bit2 |
| 4 | ATBcontrol2 | R/W | 0 | Analog Test Bus Control Bit3 |
| 3 | ATBcontrol1 | R/W | 0 | Analog Test Bus Control Bit4 |
| 2 | ATBcontrol0 | R/W | 0 | Analog Test Bus Control Bit5 |
| 1 | startMemoryBist | R/W | 0 | Set to '1' to initiate Memory built-in self test (MBIST) |
| 0 | scanTestMode | R/W | 0 | Set to 1' to enter Scan test mode. |

| | | | | |
|-------------|-------------------------|------------|------------|---|
| 7Ah | shutDownPassword | | | Set to 42h to prevent the safety critical shutdown logic from disabling the Laser when a hardware fault is detected (see also txControl0). |
| Type | R/W | PoR | 00h | |

| | | | | |
|------------------|-----------------|------------|------------|-----------|
| 7Bh - 7Eh | reserved | | | -- |
| Type | R | PoR | 00h | |

| | | | | |
|------|-------------|-----|-----|---|
| 7Fh | tableSelect | | | Indirect addressing for register tables. 00h selects the SFF-8472 Diagnostics and user EEPROM register tables. 03h selects the PHY1076-01 Device settings table. Note that data read from this register is not valid. |
| Type | R/W | PoR | 00h | |

| | | | | |
|-----------|----------|-----|-----|----|
| 80h – A7h | reserved | | | -- |
| Type | R | PoR | 00h | |

| | | | | |
|----------|------------|-----|-----|--|
| A8h– D4h | currentLUT | | | Modulation current vs. temperature Look-up table (LUT). The 45 entry LUT is indexed using the temperatureADC as follows: $(\text{temperatureADC} \times 45) / 255$. |
| Type | R/W | PoR | 00h | |

| | | | | |
|------|----------------------|-----|-----|---|
| D5h | modulationDACDefault | | | Controls the modulation current (DAC) when the LUT is disabled. During power up, the temperature is sampled and the DAC is re-loaded with a value from the LUT. |
| Type | R/W | PoR | 00h | |

| | | | | |
|-----|-------------|------|-----|--|
| D6h | txPowerDown | | | Selectively turns off the power supply to circuits in the transmitter module. '0' = power on. '1' = power off. |
| Bit | Field name | Type | PoR | |
| 7 | VDDmeaspwr | R/W | 0 | - |
| 6 | TERMpwr | R/W | 0 | - |
| 5 | DACpwr | R/W | 0 | Power down DAC |
| 4 | DRIVERpwr | R/W | 0 | Power down Laser driver |
| 3 | TXBIASpwr | R/W | 0 | Power down transmit bandgap bias + current gen. (This will completely disable the IC). |
| 2 | DBuffApwr | R/W | 0 | Power down data buffer |
| 1 | TEMPpwr | R/W | 0 | Power down temperature sensor |
| 0 | SAFETYpwr | R/W | 0 | Power down SAFETY logic |

| | | | | |
|----------|-----------|-----|-----|----|
| D7h- DAh | undefined | | | -- |
| Type | R | PoR | 00h | |

| DBh | rxPowerDown | | | Selectively turns off the power supply to circuits in the receiver module. '0' = power on. '1' = power off. |
|-----|-------------|------|-----|---|
| Bit | Field name | Type | PoR | |
| 7 | LIMITpwrđ | R/W | 0 | Power down limiter |
| 6 | FILTpwrđ | R/W | 0 | Power down RX filter |
| 5 | COMPSpwrđ | R/W | 0 | ADC Comparator powerdown |
| 4 | AMPDETPwrđ | R/W | 0 | Power down amplitude detector |
| 3 | REGpwrđ | R/W | 0 | Power down regulator |
| 2 | AGCPwrđ | R/W | 0 | Power down AGC amp |
| 1 | CMLpwrđ | R/W | 0 | Power down CML (RX related) |
| 0 | RXBIASpwrđ | R/W | 0 | Power down receiver bandgap bias + current gen. |

| DCh-DEh | undefined | | | -- |
|---------|-----------|-----|-----|----|
| Type | R | PoR | 00h | |
| | | | | |

| DFh | txControl0 | | | Control bits for the transmitter circuits. |
|-----|-----------------|------|-----|--|
| Bit | Field name | Type | PoR | |
| 7 | Osc_Mon | R/W | 0 | Multiplexes the internal oscillator onto TX_FAULT pin for monitoring (oscillator = '1', normal operation = '0') |
| 6 | Hardware_ignore | R/W | 0 | Soft Disable for Safety Critical Shutdown. Set to '1' to prevent Laser shutdown when the SCS circuits detect an electrical fault and asserts a tx fault condition. |
| 5 | ModLUTdisab | R/W | 0 | Modulation Current LUT loop control (disable LUT = '1') |
| 4 | SFTtxfault | R/W | 0 | (Internal use only. Set to '0'.) This bit is internally updated and overwritten by the watchdog counter and is not intended to be used as a software Tx Fault assert function by an external host. Use E1h bit 7 for this purpose. |
| 3 | DAC_ready | R/W | 0 | (Internal use only. Set to '0'.) |
| 2 | testBW | R/W | 0 | (Internal use only. Set to '0'.) |
| 1 | Loop_BW | R/W | 0 | Controls the average power control loop response. Set to '0' for critical damping. |
| 0 | MPC_polarity | R/W | 1 | (Internal use only. Set to '1'.) |

| E0h | | txControl1 | | Control bits for the transmitter circuits. |
|-----|-----------------|------------|-----|---|
| Bit | Field name | Type | PoR | |
| 7 | Test_comp_hiZ | R | 0 | (Internal use only. Set to '0'.) |
| 6 | Test_compout_en | R | 0 | (Internal use only. Set to '0'.) |
| 5 | Test_compout | R | 0 | (Internal use only. Set to '0'.) |
| 4 | Test_koff | R | 0 | (Internal use only. Set to '0'.) |
| 3 | SDpolarity | R/W | 1 | Controls the polarity of the SHUTDOWN pin. (For SHUTDOWN pin = 1 for shutdown, set SDpolarity = 1). |
| 2 | Kselect1 | R/W | 0 | Kselect[1:0] selects one of four gain settings for a gain stage in the automatic power control loop (see Table 4). This optimizes the loop gain for the coupling coefficient of the TOSA. |
| 1 | Kselect0 | R/W | 0 | |
| 0 | Tempsel3i | R | 0 | (Internal use only. Set to '0'.) |

| E1h | | txControl2 | | Control bits for the transmitter circuits. |
|-----|----------------|------------|-----|--|
| Bit | Field name | Type | PoR | |
| 7 | HostSFTtxfault | R/W | 0 | Set to '1' to assert a tx fault condition on the TX_FAULT pin. |
| 6 | Watchdog5 | R/W | 0 | When the watchdog counter is enabled, it must be incremented at least once every 100ms. If this does not occur then the PHY1076-01 will disable the Laser and assert a tx fault condition. Incrementing the counter or disabling the watchdog will cause normal operation to resume. |
| 5 | Watchdog4 | R/W | 0 | |
| 4 | Watchdog3 | R/W | 0 | |
| 3 | Watchdog2 | R/W | 0 | |
| 2 | Watchdog1 | R/W | 0 | |
| 1 | Watchdog0 | R/W | 0 | |
| 0 | WatchdogEn | R/W | 0 | Watchdog Function Enable (enable = 1) |

| E2h - E4h | | txControlSpare | | reserved |
|-----------|---|----------------|-----|----------|
| Type | R | PoR | 00h | |
| | | | | |

| E5h–E6h | | ddmChecksum | | 16-bit checksum updated by the PHY1076-01 every 10ms. See section 5.2.3 for a detailed description. |
|---------|---|-------------|-----|---|
| Type | R | PoR | 00h | |
| | | | | |

| E7h | diagnosticsSelect | | | Diagnostic functions (for internal use) are controlled by this register. |
|------------|--------------------------|-------------|------------|---|
| Bit | Field name | Type | PoR | |
| 7 | - | | 0 | spare |
| 6 | - | R | 0 | spare |
| 5 | - | R | 0 | spare |
| 4 | - | R | 0 | spare |
| 3 | - | R | 0 | spare |
| 2 | - | R | 0 | spare |
| 1 | wdInhibit | R/W | 0 | See also register 78h alarmBytePHY1076. Set to '1' to disable the timer and prevent the chip from resetting itself if the timer is not serviced. Set to '0' for normal operation. |
| 0 | tstcksel | R/W | 0 | Set to '1' to select the SA_SDA pin as the clock source for the digital macro instead of the internal oscillator. |

| E8h | rxControl0 | | | Control bits for the receiver circuits. |
|------------|--------------------|-------------|------------|---|
| Bit | Field name | Type | PoR | |
| 7 | AMPDET_dcfbdisable | R | 0 | (Internal use only. Set to '0'.) |
| 6 | Gc_disable | R | 0 | (Internal use only. Set to '0'.) |
| 5 | AGCdcfb_disable | R | 0 | (Internal use only. Set to '0'.) |
| 4 | Trimsel | R/W | 0 | (Internal use only. Set to '0'.) |
| 3 | RX_dccouple | R/W | 0 | For AC coupled input, set to '0' to terminate the differential signal at RXIN+/- to a common mode voltage. Set to '1' when the inputs are DC coupled. |
| 2 | LOSpolarity | R/W | 0 | LOS pin sense ('1'=Signal Detect;'0'=Loss of signal) |
| 1 | LOStype | R/W | 0 | LOS Detection Type ('1'=OMA;'0'=Mean RX power) |
| 0 | CMLslew | R/W | 0 | RXOUT+/- slew rate control. Set to '0' for a fast slew rate. Set to '1' for slow slew rate. |

| | | | | |
|------------|-------------------|-------------|------------|--|
| E9h | rxControl1 | | | Control bits for the receiver circuits. |
| Bit | Field name | Type | PoR | |
| 7 | - | R | 0 | Spare |
| 6 | - | R | 0 | Spare |
| 5 | - | R | 0 | Spare |
| 4 | LorV | R | 0 | Always set to '1' for laser operation |
| 3 | Fosctrim1 | R | 0 | (Internal use only. Set to '0'.) |
| 2 | Fosctrim0 | R | 0 | (Internal use only. Set to '0'.) |
| 1 | HiLoSwing | R/W | 0 | Controls the differential swing of the signal output on RXOUT+/- ('1' = high amplitude, '0' = low amplitude) |
| 0 | LIM_dcfbdisable | R | 0 | (Internal use only. Set to '0'.) |

| | | | | |
|------------------|-----------------------|------------|------------|----------|
| EAh - EFh | rxControlSpare | | | reserved |
| Type | R | PoR | 00h | |

| | | | | |
|-------------|------------------|------------|------------|----|
| F0h | undefined | | | -- |
| Type | R | PoR | 00h | |

| | | | | |
|-------------|-------------|------------|------------|--|
| F1h | Vref | | | Reference voltage trim DAC. The reference voltage can be set by adjusting Vref until the desired voltage is seen at pin RREF. RREF is pulled to ground by a 10 KΩ resistor for a 1V reference. |
| Type | R/W | PoR | 71h | |

| | | | | |
|-------------|---------------------|------------|------------|--|
| F2h | tx_power_set | | | Sets the Tx mean power DAC. This DAC therefore controls the average output power of the Laser. |
| Type | R/W | PoR | 00h | |

| | | | | |
|-------------|--------------------|------------|------------|---|
| F3h | OMA_LOS_set | | | Sets the threshold level for optical measurement amplitude based LOS detection. |
| Type | R/W | PoR | 00h | |

| | | | | |
|-------------|--------------------|------------|------------|---|
| F4h | AVG_LOS_set | | | Sets the threshold level for receiver signal strength indicator (RSSI) based LOS detection. |
| Type | R/W | PoR | 00h | |

| | | | | | |
|------------|-------------------|-------------|------------|--|--|
| F5h | rateSel | | | Controls the bandwidth of the programmable low pass filter in the receiver. The two rate selection fields A and B enable switching between two different bandwidths using the RATESEL pin. | |
| Bit | Field name | Type | PoR | | |
| 7 | TRIM1 | R/W | 0 | | (Internal use only. Set to '0'.) |
| 6 | TRIM0 | R/W | 0 | | (Internal use only. Set to '0'.) |
| 5 | RateselB2 | R/W | 0 | | Rate Selection B. Selects one of six cut-off frequency settings (see Table 1). |
| 4 | RateselB1 | R/W | 0 | | |
| 3 | RateselB0 | R/W | 0 | | |
| 2 | RateselA2 | R/W | 0 | | Rate Selection A. Selects one of six cut-off frequency settings (see Table 1). |
| 1 | RateselA1 | R/W | 0 | | |
| 0 | RateselA0 | R/W | 0 | | |

| | | | | |
|-------------|--------------------|------------|------------|--|
| F6h | txDriverCap | | | Selects between different time constants for the trimming network which controls the tx driver output damping (see Table 5). |
| Type | R/W | PoR | 00h | |

| | | | | |
|----------------|-----------------|------------|------------|----|
| F7h-FAh | reserved | | | -- |
| Type | R | PoR | 00h | |

| | | | | |
|-------------|-------------------|------------|------------|--|
| FBh | rxPowerADC | | | This register is dual functioned. Reads received optical power, Rx ADC value. Writes data integrity value SerialEepromIdentifier0. |
| Type | R/W | PoR | 00h | |

| | | | | |
|-------------|------------------|------------|------------|---|
| FCh | txBiasADC | | | This register is dual functioned. Reads Laser bias, Tx Bias ADC value. Writes data integrity value SerialEepromIdentifier1. |
| Type | R/W | PoR | 00h | |

| | | | | |
|-------------|-------------------|------------|------------|--|
| FDh | txPowerADC | | | This register is dual functioned. Reads transmit optical power, Tx Power ADC value. Writes data integrity value SerialEepromIdentifier2. |
| Type | R/W | PoR | 00h | |

| | | | | |
|-------------|-----------------------|------------|------------|--|
| FEh | temperatureADC | | | This register is dual functioned. Reads module temperature ADC value. Writes data integrity value SerialEepromChecksum0. |
| Type | R/W | PoR | 00h | |

| | | | | |
|-------------|---------------|------------|------------|--|
| FFh | vddADC | | | This register is dual functioned. Reads power supply, VDD ADC value. Writes data integrity value SerialEepromChecksum1. |
| Type | R/W | PoR | 00h | |

7. Simplified Interface Models

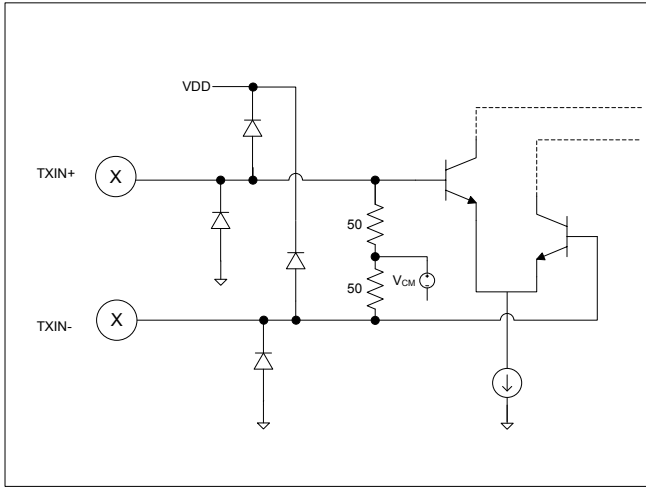


Figure 30- Transmit input structure

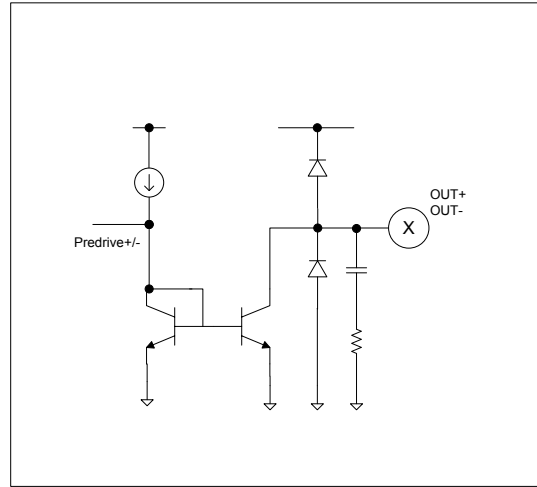


Figure 31- Transmit output structure

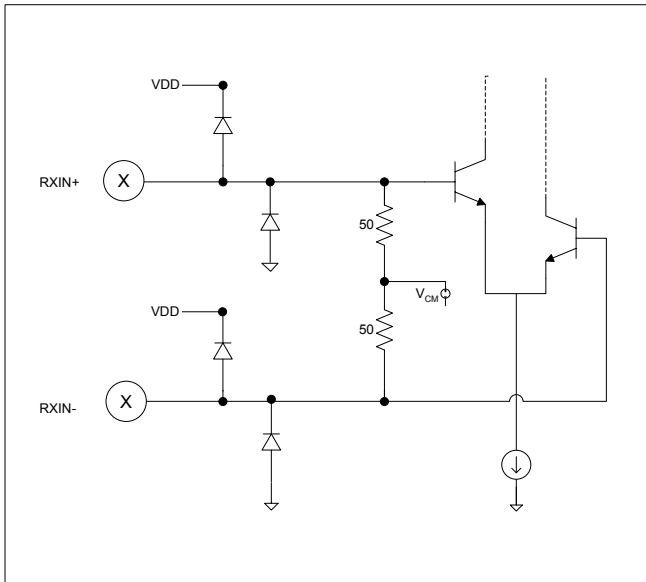


Figure 32- Receive input structure

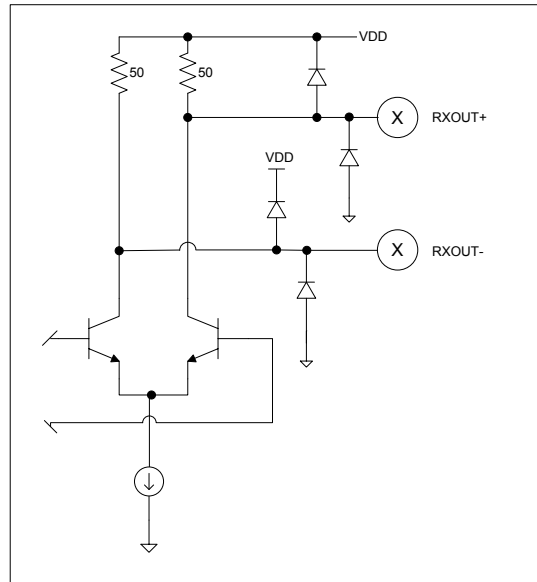


Figure 33- Receive output structure

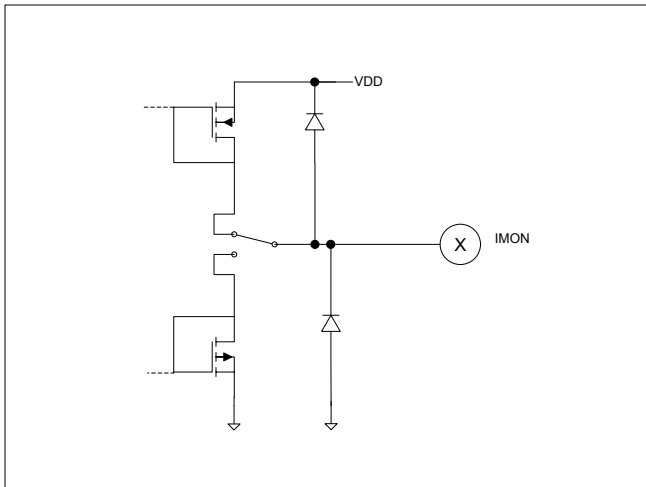


Figure 34- MPD input structure

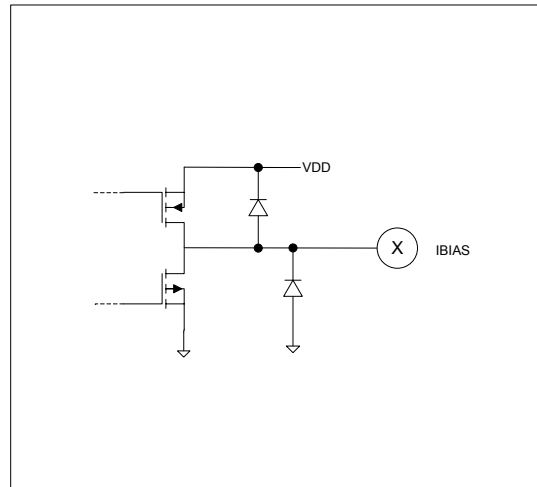


Figure 35- Laser bias output structure

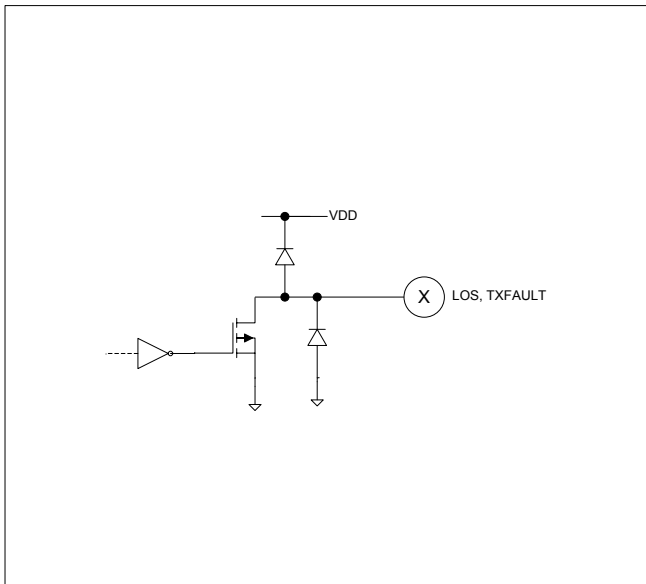


Figure 36- LOS/TX_FAULT output

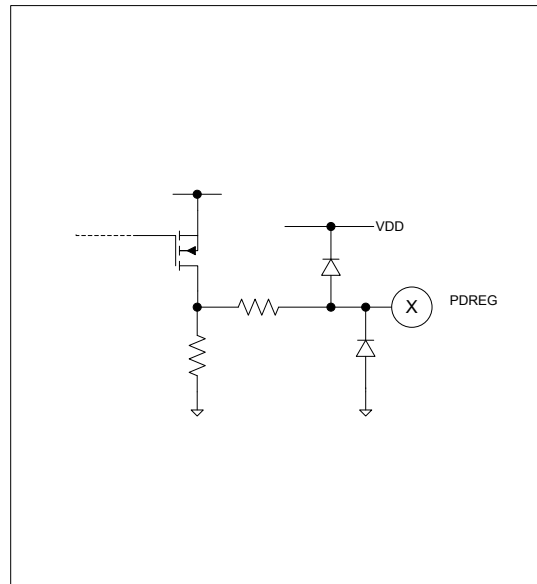


Figure 37- RSSI regulator output structure

8. Typical Applications

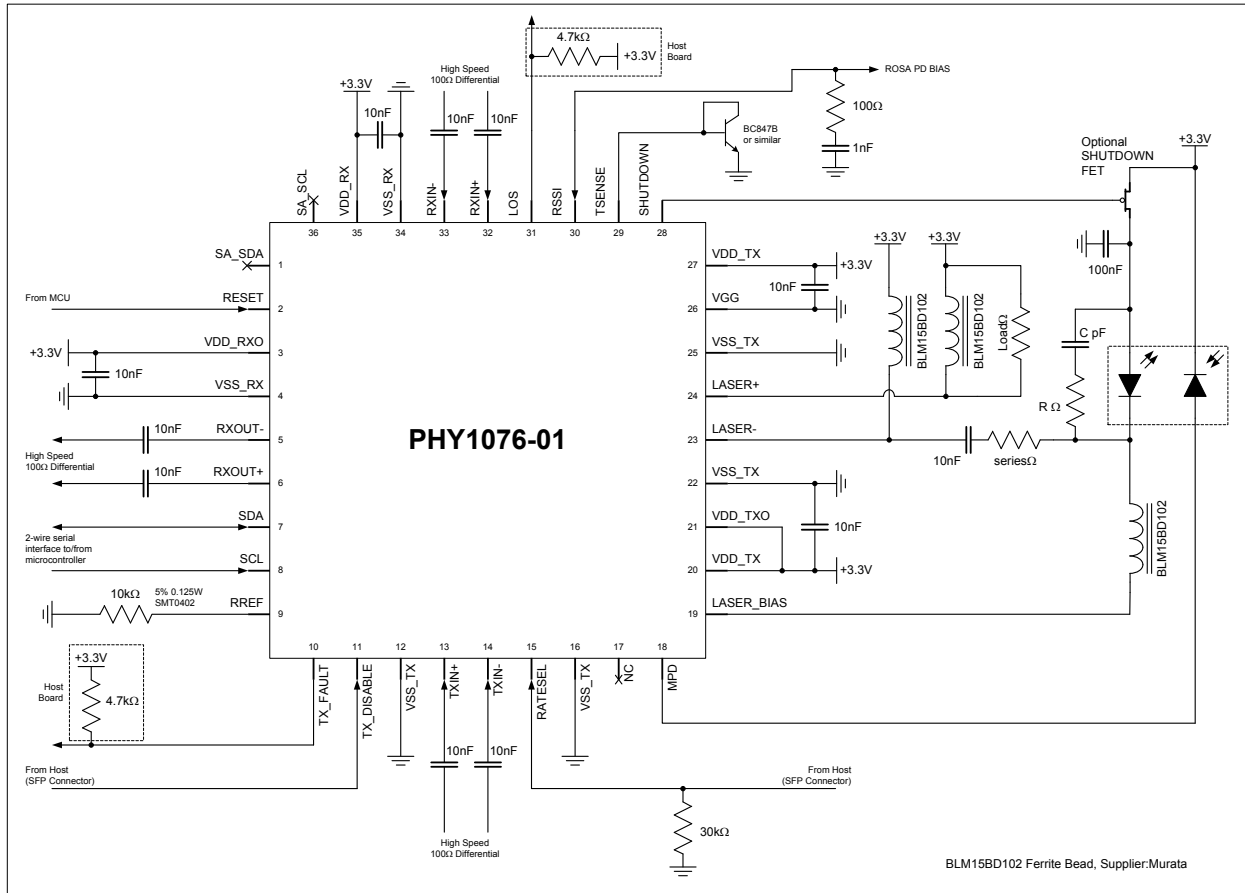


Figure 38 – PHY1076-01 in DDM Mode

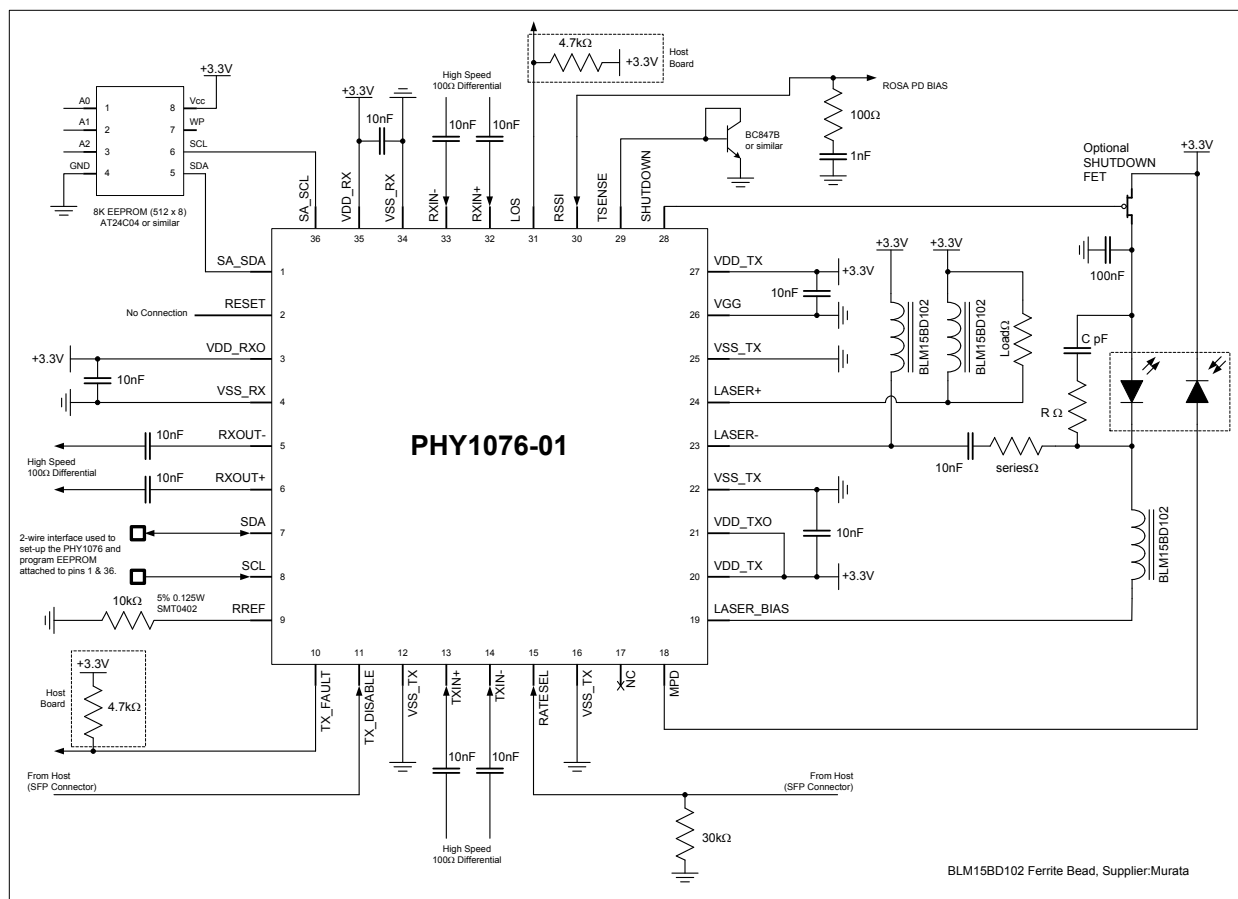


Figure 39 – PHY1076-01 in Stand-alone Mode

8.1. Power Supply Connections

The PHY1076-01 has been designed as a low power device. In order to achieve low operating power consumption the transmitter and receiver circuitry in the PHY1076-01 share some common internal bias circuitry. This requires that the PHY1076-01 transmitter and receiver be powered up together for correct operation. Powering up the transmitter VDDs and not the receiver VDDs, or the reverse, will not damage the PHY1076-01 but will cause the part to function incorrectly.

8.1.1. Power Supply Filtering

Although the Tx VDDs and Rx VDDs should be powered together and therefore, ultimately be connected at a common node, it is beneficial to separately filter the power supplies for the Tx VDD and Rx VDD supplies. Separately filtering the transmitter and receiver supplies off chip will reduce power supply noise and cross talk between the transmitter and receiver – it is generally good practice to separately filter and decouple the individual supplies on any multifunction IC.

In addition to supplying separately filtered supplies to the Tx VDDs and Rx VDDs of the PHY1076-01, it is also recommended that any other ICs and digital circuitry connected to the PHY1076-01 in an application environment (e.g. SFP module) be suitably filtered and decoupled also. An example of this would be to supply a filtered digital supply for the external MCU, required to compliment the PHY1076-01 in DDM SFF-8472 applications.

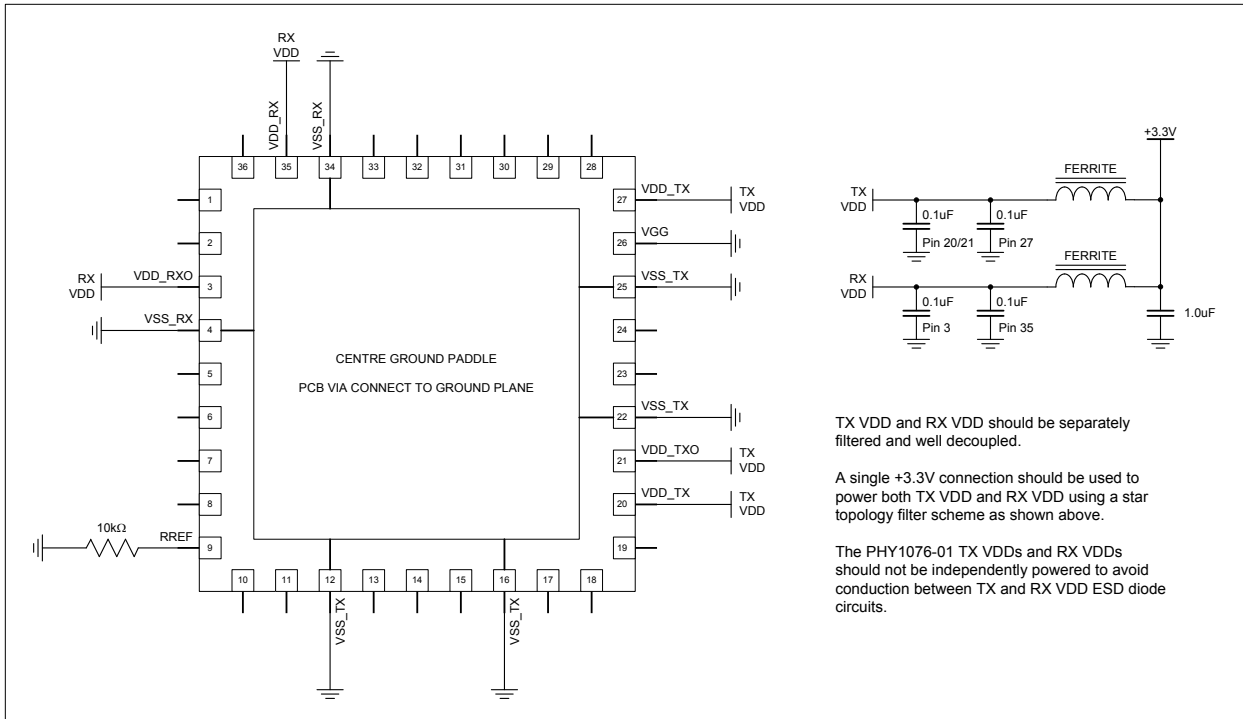


Figure 40 – Recommended power supply connections and filtering.

8.1.2. Power-On-Reset

The PHY1076-01 features an internal power-on-reset function that applies a reset to the digital logic once the supply voltage reaches a preset value (>2.0V). The internal power-on-reset typically takes 27ms after power has been applied based on a 50ms slow start voltage ramp. The PHY1076-01 may be reset externally by applying a logic low pulse to the reset pin which is internally pulled up. This is useful to guarantee the state of the PHY1076-01 logic when using the device in conjunction with an external MCU.

9. Packaging

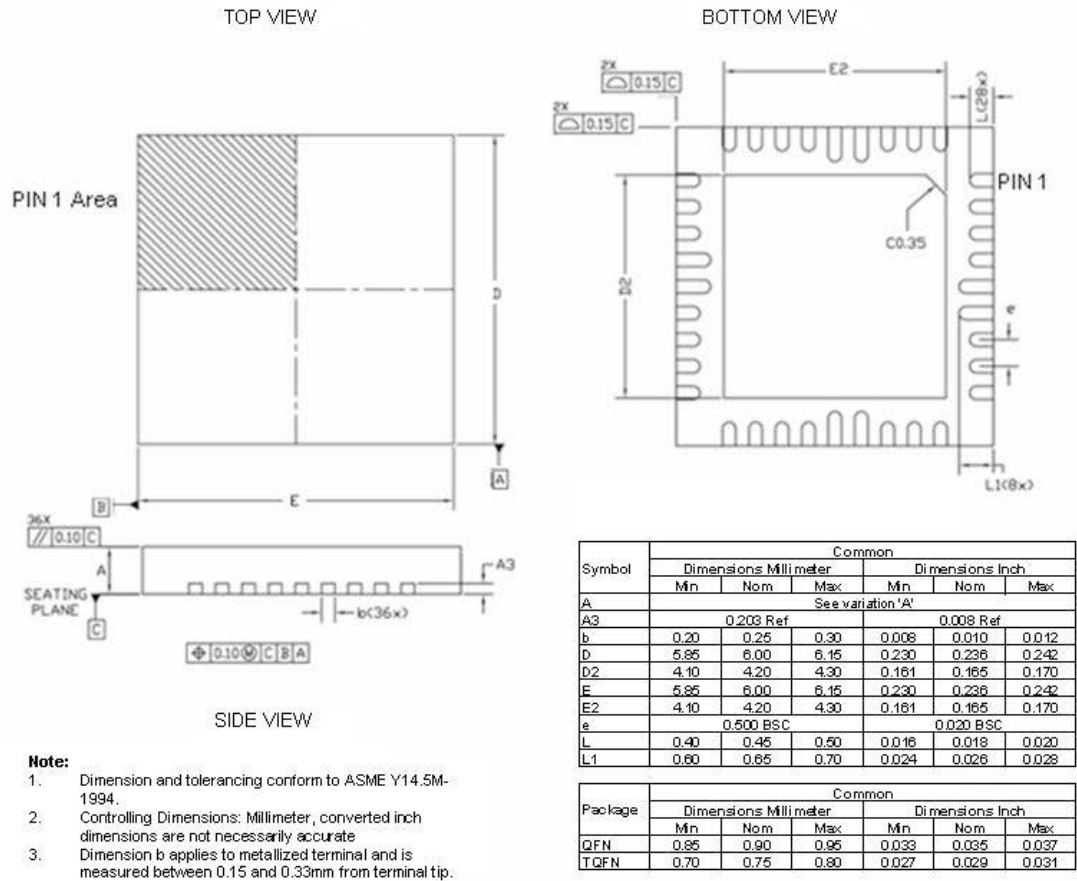


Figure 41 - QFN 36 Package Outline Drawing

10. Contact Information

For technical support, contact Maxim at www.maximintegrated.com/support.