AN3031
Application note

SCLT3-8 input termination demonstration board
STEVAL-IFP007V1

1 Introduction

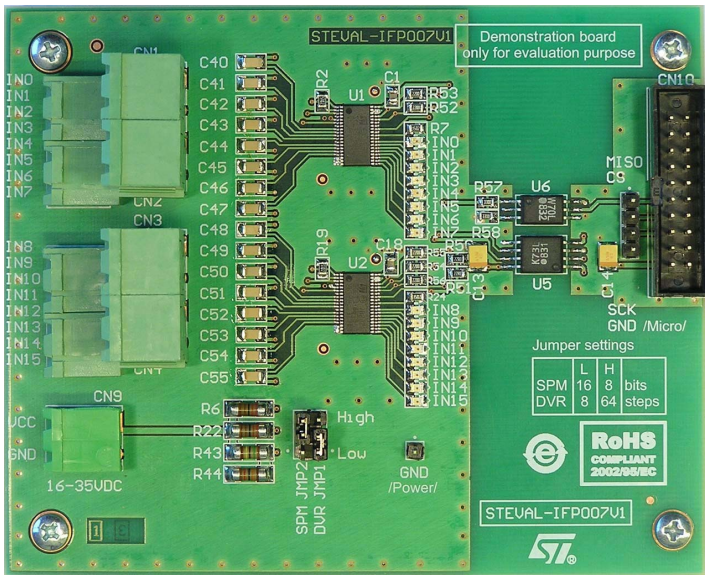
The SCLT3-8BT8 is an eight channel termination used for interfacing automation digital inputs. It is designed for 24 VDC applications and meets type 3 input characteristics in accordance with IEC 61131-2 (programmable controllers international standard). The chip integrates an SPI peripheral output for communication with logic/ASIC/microcontroller. Its structure allows the transfer not only of the data but also of additional information including thermal alarm, undervoltage indication and parity bits. It is particularly beneficial for applications with high channel counts. The serial communication allows for reduction of the number of lines, which in most applications need to be galvanically isolated.

The device optimizes the input VI characteristic shape to reduce power dissipation. This becomes critical when the application enclosure requires higher protection levels, such as IP codes IP65 and IP67. These closed cabinets are used in various automated lines, including the food industry. The power dissipated inside the module is very limited, as there is usually no air circulation inside the box. The current limitation also reduces power losses on the sensor side.

Another important parameter is electrical protection and susceptibility of the application. The SCLT3-8BT8 implements large protection diodes on each input and supply voltage line. Serial resistors ensure a higher level of susceptibility than required.

Thanks to its compact package, an SCLT3-8BT8 application occupies little space on the PCB compared to discrete solutions.

Figure 1. STEVAL-IFP007V1 demonstration board



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2 Description

The STEVAL-IFP07V1 demonstration board is an application intended to allow designers to evaluate the behavior of the SCLT3-8BT8 device in industrial environmental conditions. The board accommodates two SCLT3-8BT8 chips connected to the SPI bus in a daisy chain configuration. It offers a 16-bit digital input interface and indicates each sensor logic state with an LED.

Features

- 8/16 input channel topology (SCLT3-8BT8 chip / STEVAL-IFP007V1 board)
- Fully integrated current limiter
- Termination for IEC 61131-2 type 1 and 3 inputs
- Digital filter on each input
- SPI communication peripheral
- Voltage regulator integrated on the chip
- Thermal alarm
- Wide range supply voltage operation

Benefits

- Low power dissipation compared to discrete solutions
- Small external component count
- Overvoltage protection
- ESD in accordance with IEC 61000-4-2, class 3, 8 kV air discharge, 6 kV contact discharge
- Excellent EMC immunity
  - High energy surge (IEC 61000-4-5), 2 kV / criteria “B” (42 Ω / 0.5 µF) without any Transil™ protection
  - Fast transient burst (IEC 61000-4-4), +4 kV / –8 kV (±8 kV[a]) / criteria “A”
  - RF amplitude modulation (IEC 61000-4-6), 150 kHz - 80 MHz, 10 V / criteria “A”
- Cost-effective isolation thanks to an SPI bus
- Reduces overall dissipation
- Compact module HTSSOP-38 package

a. With 10 pF capacitive GND coupling (primary vs. secondary ground of the isolation).

2.1 SCLT3-8BT8

The SCLT3-8BT8 (current limited termination) is an eight-channel digital input termination device designed for 24 VDC automation applications. Typical applications for this device include PLCs (programmable logic controllers), PACs (programmable automation controllers), distributed I/O systems, etc. The device works as an interface for mechanical switches, relay contacts and two-wire or three-wire digital sensors (also known as proximity switches).

Available in eight-channel configuration, it offers a high-density termination by minimizing the external component count. It is housed in a HTSSOP-38 surface mount package to reduce the printed circuit board size.

The chip consists of a parallel input voltage protection circuit, a current limiting circuit which regulates the channel current and feeds the indicator LEDs, a digital filter to prevent glitches, a voltage regulator and SPI communication peripheral.

The SCLT3-8BT8 device is connected between the sensors and the application microcontroller, FPGA or ASIC. The current limiting circuit is compensated over the entire temperature range. Thanks to its low tolerance, the current limitation allows drastic reduction of dissipation compared to a resistive input (discrete solution) - the overall module requires less cooling capability and is smaller.

Thanks to integrated SPI communication, the solution reduces the number of lines which typically need to be galvanically isolated, making the application more cost-effective. In a 16-bit input interface, conventional solutions require 16 isolators to decouple the control part from an industrial environment. With the SCLT3-8BT8, the two-chip solution (16-bit interface) connected in a daisy chain configuration requires only 3 isolators. In addition to the input data, it also provides device status information including thermal alarm, undervoltage indication, and others. Parity check bits for higher reliability are also included in the frame extension.

The SCLT3-8BT8 device principal block diagram and recommended application structure is provided in *Figure 2* and *Figure 3*.

Figure 2. SCLT3-8BT8 block diagram

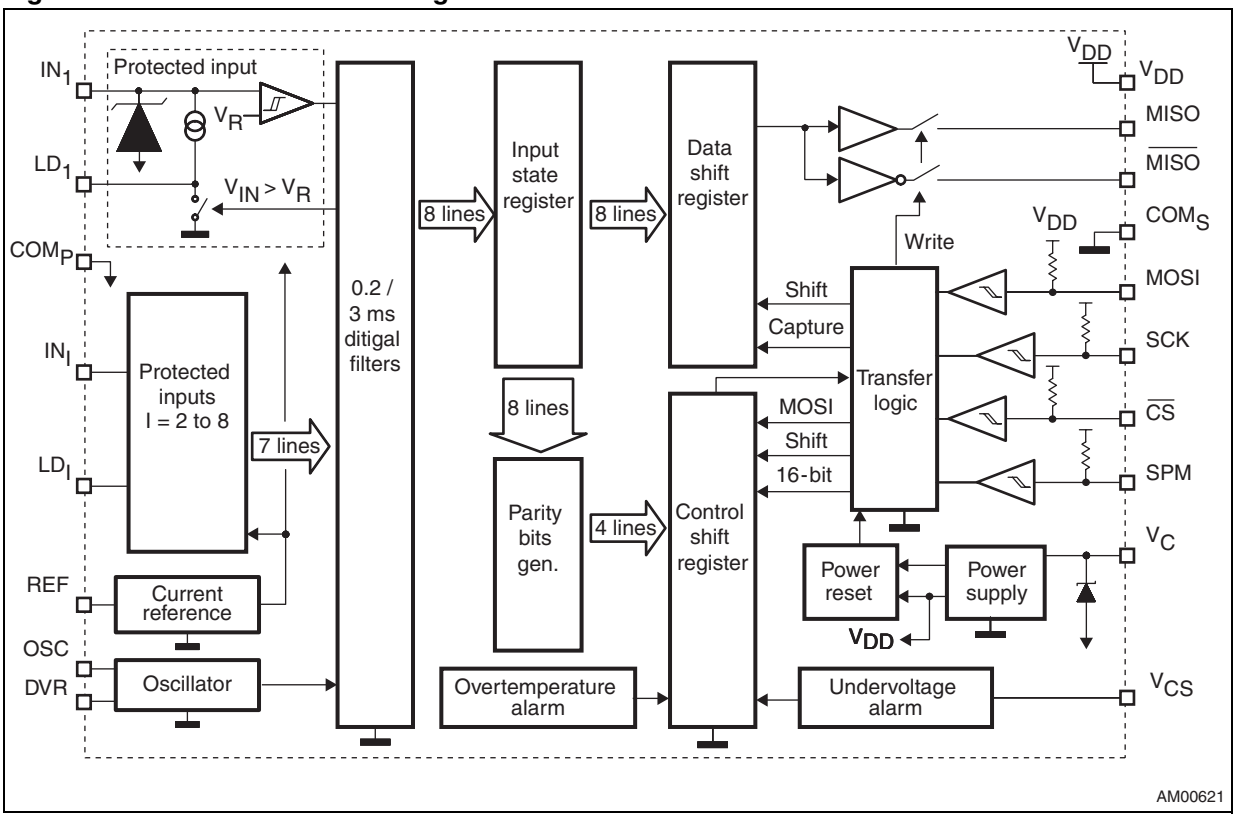
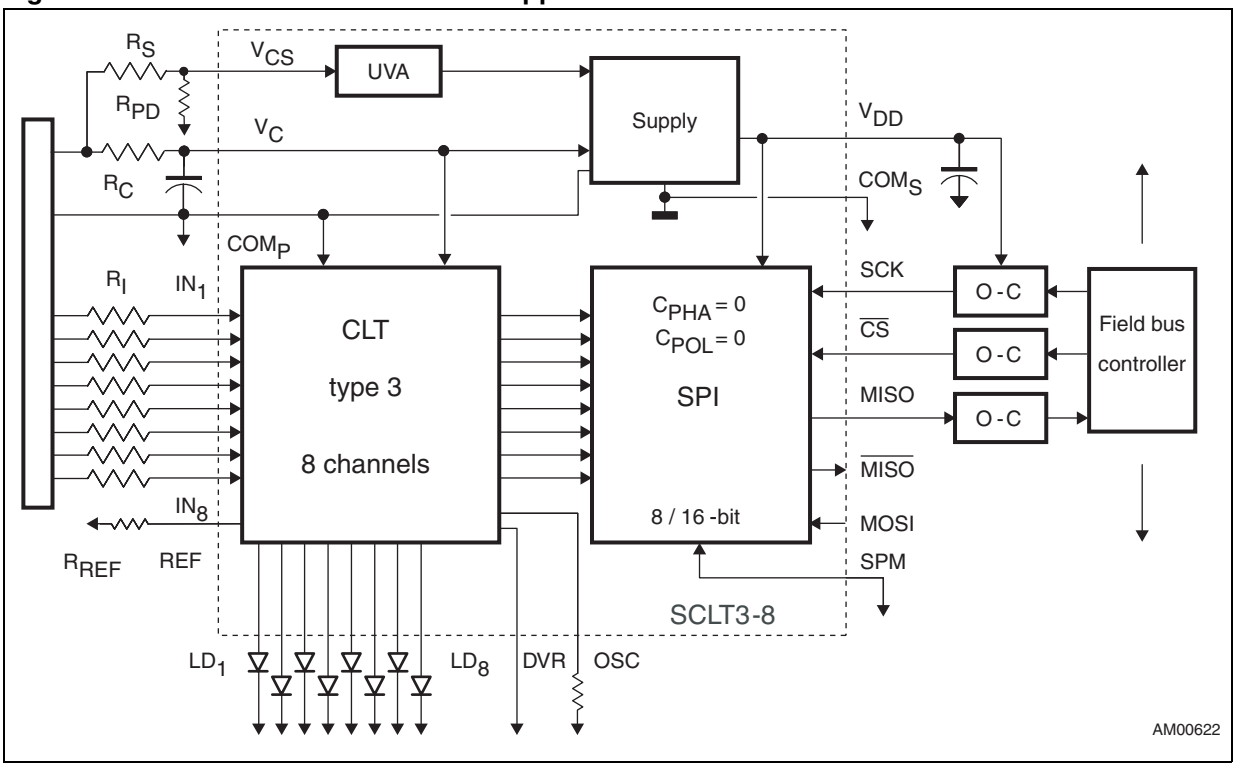


Figure 3. SCLT3-8BT8 recommended application structure



2.2 STEVAL-IFP007V1 demonstration board

The STEVAL-IFP007V1 connection diagram is provided in *Figure 4*, *5* and *6*. It is compliant with type 1 and 3 input characteristics in accordance with the IEC 61131-2 standard. The application is typically supplied from two sides using two independent power supplies - primary and secondary. The primary power supply has a typical voltage of 24 VDC (functional range from 16 to 35 VDC), and is connected to the CN9 terminal. The secondary supply is connected through the CN10 (SPI) socket. This supply voltage level derives from the microcontroller or control logic supply voltage. It is considered within range from 3 VDC up to 5 VDC. For immunity considerations, the board design is optimized for 5 V signal levels. If interconnection of the board with 3 V or 3.3 V logic is required, resistors R48, R49, R59 and R60 should be replaced by a value of approximately 160 Ω

Special attention should be given top the input and supply line resistors (R_I, R_C). Their type dramatically influences the application's EMC - high voltage surge robustness (IEC 61000-4-5). The resistors should be capable of sustaining high peak voltage and current levels. A suitable type is, for example, the MELF MMB0207 from VISHAY®. Peak ratings of such resistors are 70 W, or 3 kV. Standard SMD 1206 resistors are not recommended, as their rating are much lower. Therefore, the application fails at surge levels close to 1 kV (differential mode, 42 Ω / 0.5 µF coupling).

Each SCLT3-8BT8 input signal is additionally filtered with a capacitor of 1 nF. These components increase capacitive coupling to the GND reference and therefore maximize EFT immunity. The capacitor values can be increased to 22 nF, for example, to achieve even higher immunity levels, but with the drawback of bandwidth limitation.

Each SPI signal (CS, SCK, and MOSI) is filtered close to each SCLT3-8BT8 chip with an integration R-C cell which limits the bandwidth to suppress noise sensitivity. Values used in the application are 220 Ω - 100 pF, which correspond to the maximum communication baud rate of approximately 3 Mbps. It is up to the application designer to set the appropriate R-C values in order to suppress high frequency noise. Naturally, increasing the capacitor values renders the signals more stable, which has a positive effect on the immunity, but the communication bandwidth is lower.

Figure 4. Application connection diagram - part 1

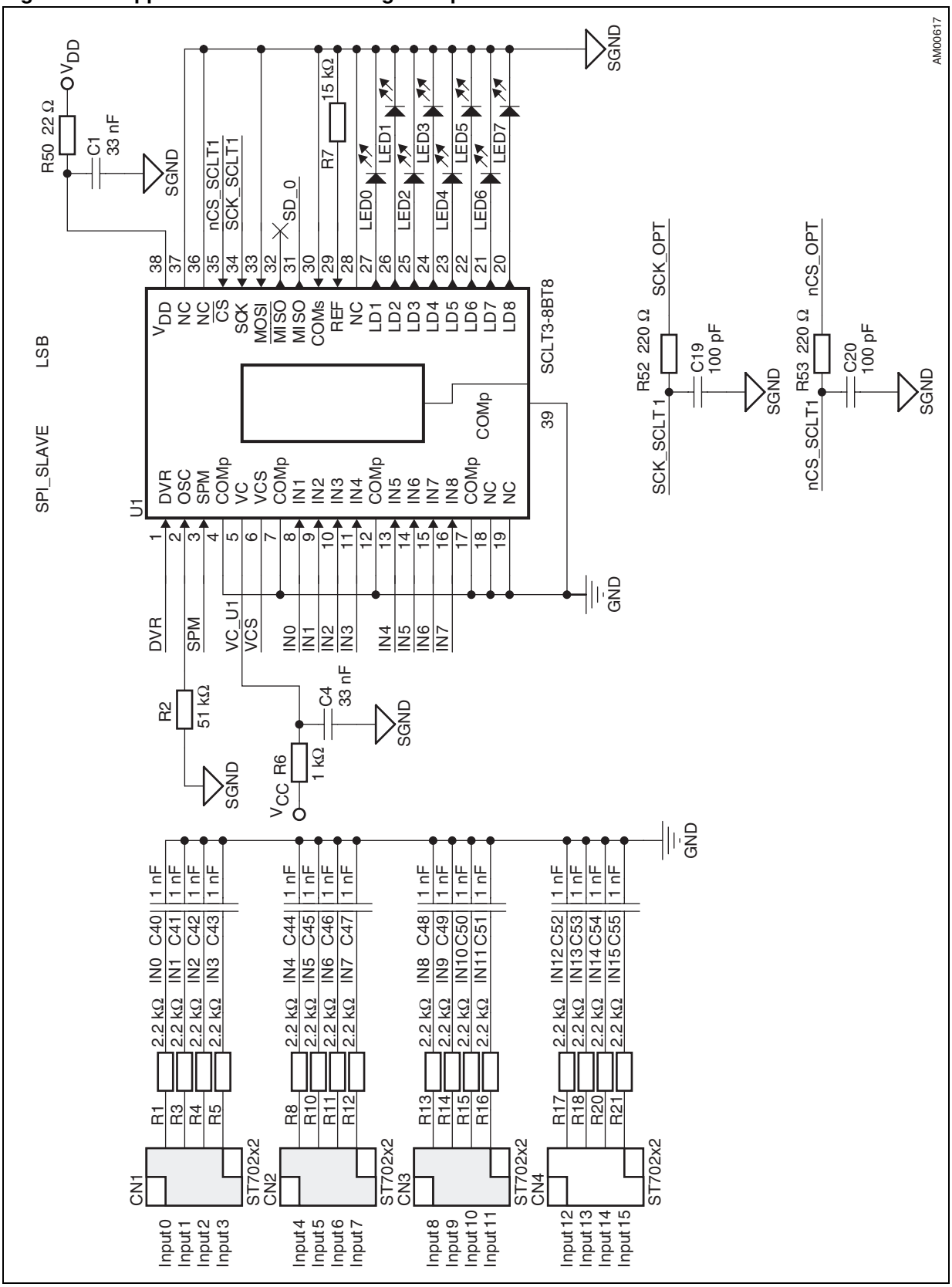


Figure 5. Application connection diagram - part 2

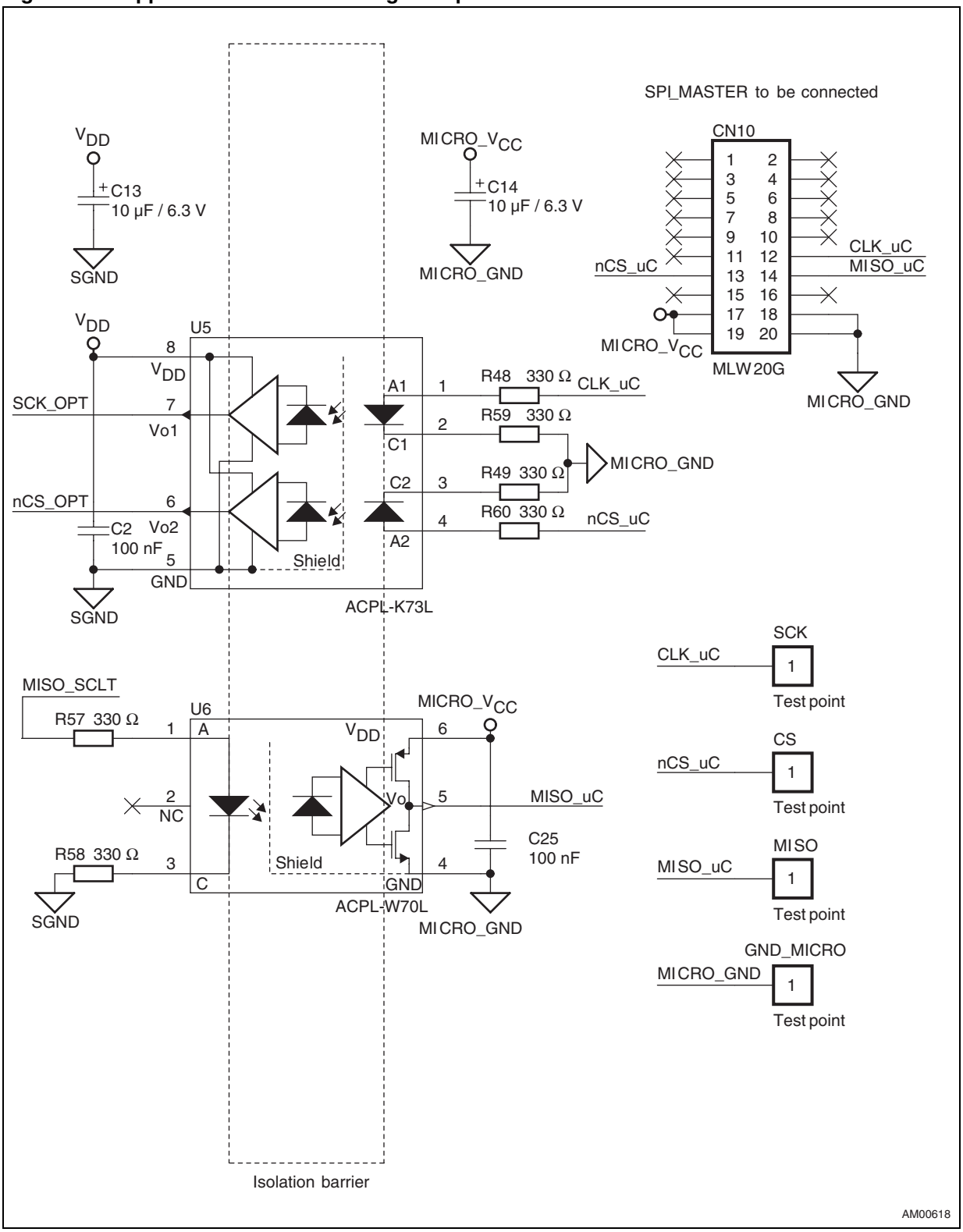


Figure 6. Application connection diagram - part 3

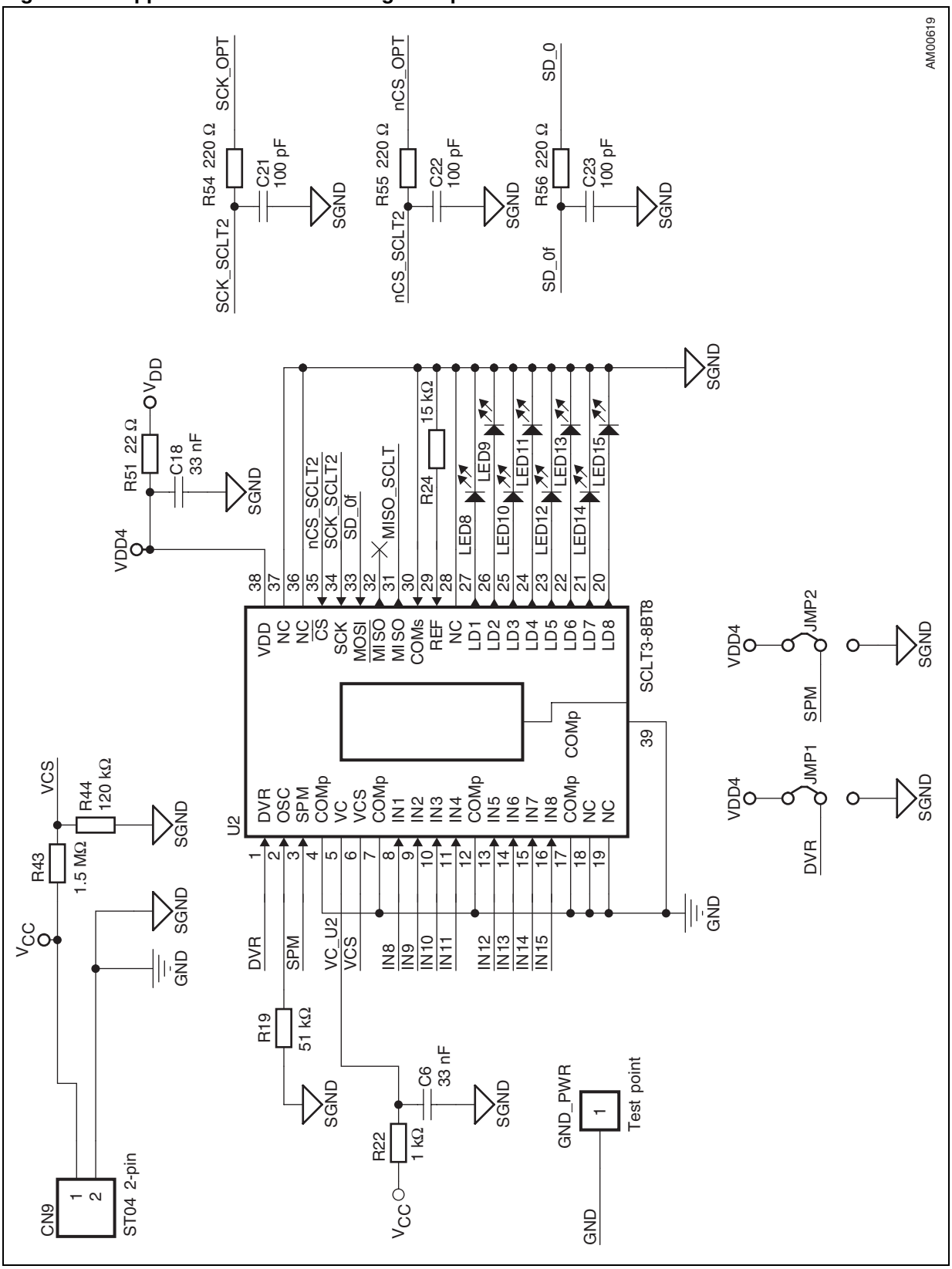


Table 1. Bill of material

Designator	Qty	Comment	Description	Footprint
C1, C4, C6, C18	4	33 nF	Ceramic capacitor	SMD 0805
C2, C25	2	100 nF	Ceramic capacitor	SMD 0805
C13, C14	2	10 µF / 6.3 V	Tantalum capacitor	SMD 1210
C19, C20, C21, C22, C23	5	100 pF	Ceramic capacitor	SMD 0805
C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55	16	1 nF	Ceramic capacitor	SMD 1206
CN1, CN2, CN3, CN4	4	MDSTB 2,5/ 2-G-5,08	Terminal block - Phoenix Contact	THT
CN1_Plug, CN2_Plug, CN3_Plug, CN4_Plug	4	MSTB 2,5/ 4-ST-5,08	Terminal block - Phoenix Contact	THT
CN9	1	MSTB 2,5/ 2-G-5,08	Terminal block - Phoenix Contact	THT
CN9_Plug	1	MSTB 2,5/ 2-ST-5,08	Terminal block - Phoenix Contact	THT
CN10	1	MLW20G	Header, 10-pin, dual row, with key	THT
CS, GND_MICRO, GND_PWR, MISO, SCK	5	Test point	Header, 1-pin	THT
JMP1, JMP2	2	Header	Header 2-pins / 2.54 mm for jumper	THT
JMP1_Socket, JMP2_Socket	2	Jumper	Jumper 2.54 mm	THT
LED0, LED1, LED2, LED3, LED4, LED5, LED6, LED7, LED8, LED9, LED10, LED11, LED12, LED13, LED14, LED15	16	LED SMD	Green LED	SMD 0805
R1, R3, R4, R5, R8, R10, R11, R12, R13, R14, R15, R16, R17, R18, R20, R21	16	2.2 kΩ	Resistor - high peak power	SMD MELF 0207
R2, R19	2	51 kΩ	Resistor	SMD 0805
R6, R22	2	1 kΩ	Resistor - high peak power	SMD MELF 0207
R7, R24	2	15 kΩ	Resistor	SMD 0805
R43	1	1.5 MΩ	Resistor - high peak power	SMD MELF 0207
R44	1	120 kΩ	Resistor - high peak power	SMD MELF 0207
R48, R49, R57, R58, R59, R60	6	330 Ω	Resistor	SMD 0805
R52, R53, R54, R55, R56	5	220 Ω	Resistor	SMD 0805
R50, R51	2	22 Ω	Resistor	SMD 0805
U1, U2	2	SCLT3-8BT8	Digital input termination	SMD HTSSOP 38
U5	1	ACPL-K73L	Optocoupler	SMD SO8-wide
U6	1	ACPL-W70L	Optocoupler	SMD SO6-wide

Figure 7. Demonstration board photo - top view

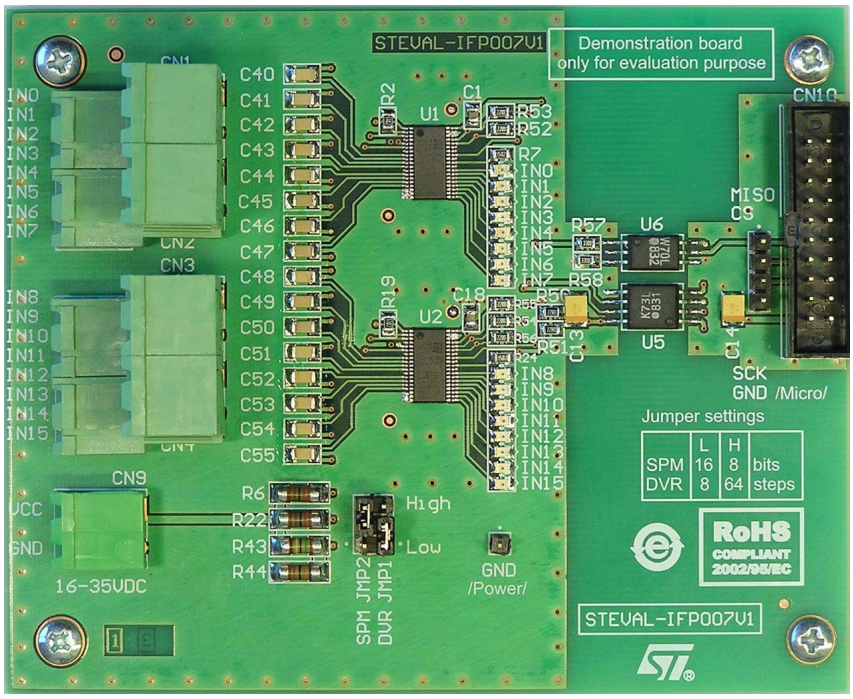
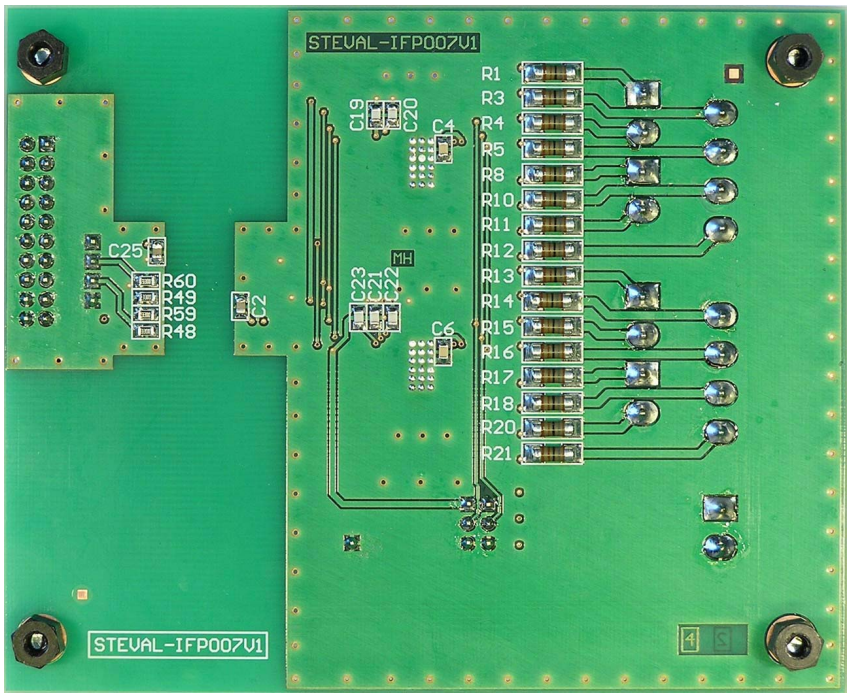


Figure 8. Demonstration board photo - bottom view



3 Demonstration board PCB layout

3.1 EMC optimal PCB considerations

The following section provides basic instructions on how to implement an EMC optimized PCB layout.

It is necessary to filter the SPI signals close to each SCLT3-8BT8 chip to prevent noise spikes that trigger the SCK, CS or influence the data line. Single integration R-C cells are sufficient. The R-C values should be chosen according to the requested baud rate. For example, given a 220 Ω resistor and a ceramic capacitor with a value of:

a) 100 pF
b) 220 pF
c) 470 pF

the corresponding maximum communication frequency in the STEVAL-IFP007V1 application structure is:

a) 3 MHz
b) 1.6 MHz
c) 870 kHz

The route length should be minimized.

The path between the input signal terminals through input resistors to the filtering capacitors should also be as short as possible. The SCLT3-8BT8 also embeds digital filters to reduce accidental pulses (or “glitches”) entering the input lines. The use of capacitive filters is recommended in addition to improve overall application EMC immunity.

The main reason is to establish a capacitive coupling between the input signals and GND (which is a reference for all the application signals on the primary side).

Practical experience with several PCB design revisions has shown that application immunity is substantially influenced by routing shape and the copper pours. Extending the board to four routing layers improved EMC performance. The outer (top and bottom) layers are used for signal routing. Moreover, they use copper pours surrounding the primary (SCLT) and secondary (microcontroller) part. The inner layers are used to distribute GND, V_{CC} and V_{REG} potentials. The layouts of the different layers are shown in Figures *9* to *12*.

The consequence of such a structure is maximized capacitive coupling between all the signals vs. GND reference. Therefore, all noise influencing any signal (input, supply voltage) is eliminated and has a common mode effect.

An empty isolation space (without routes, copper areas and components) is implemented between the primary and secondary application parts. Due to the isolator (optocoupler) sensitivity on fast common mode transitions, both application sections could be additionally coupled with high voltage ceramic capacitors. This increases overall application robustness. EMC tests show immunity increases when a 10 pF capacitor has been placed between SGND and MICRO_GND.

3.2 PCB layer set

Figure 9. Top layer PCB layout

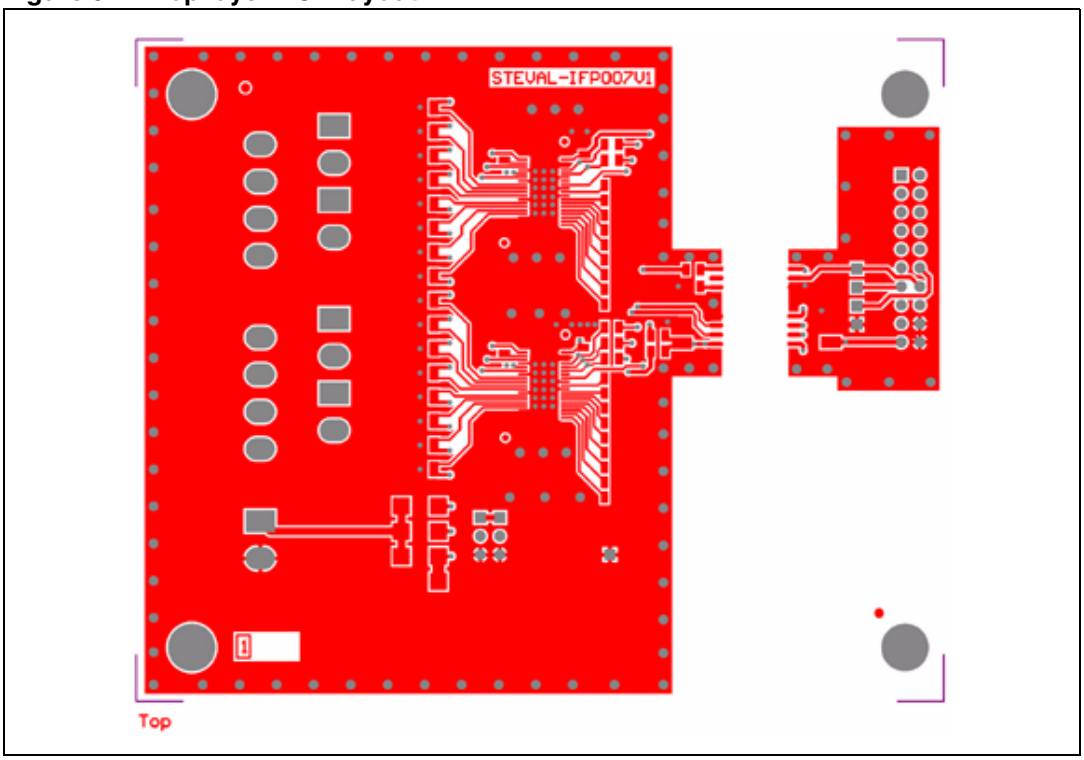


Figure 10. Top inner layer PCB layout

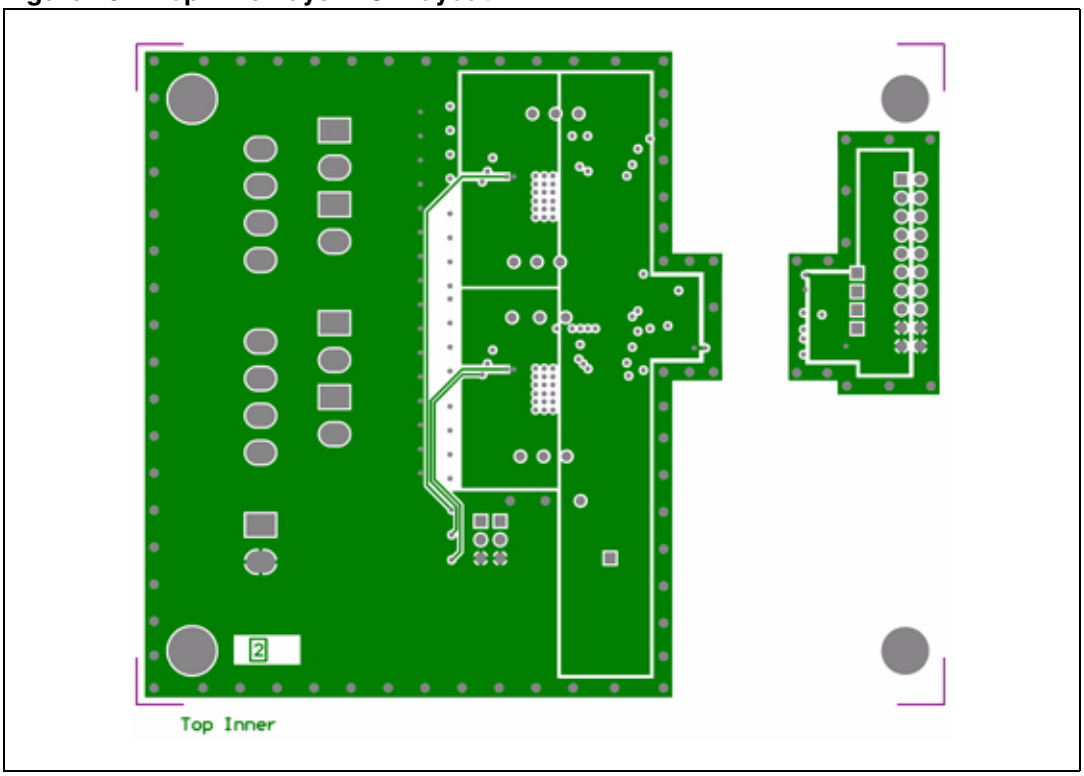


Figure 11. Bottom inner layer PCB layout

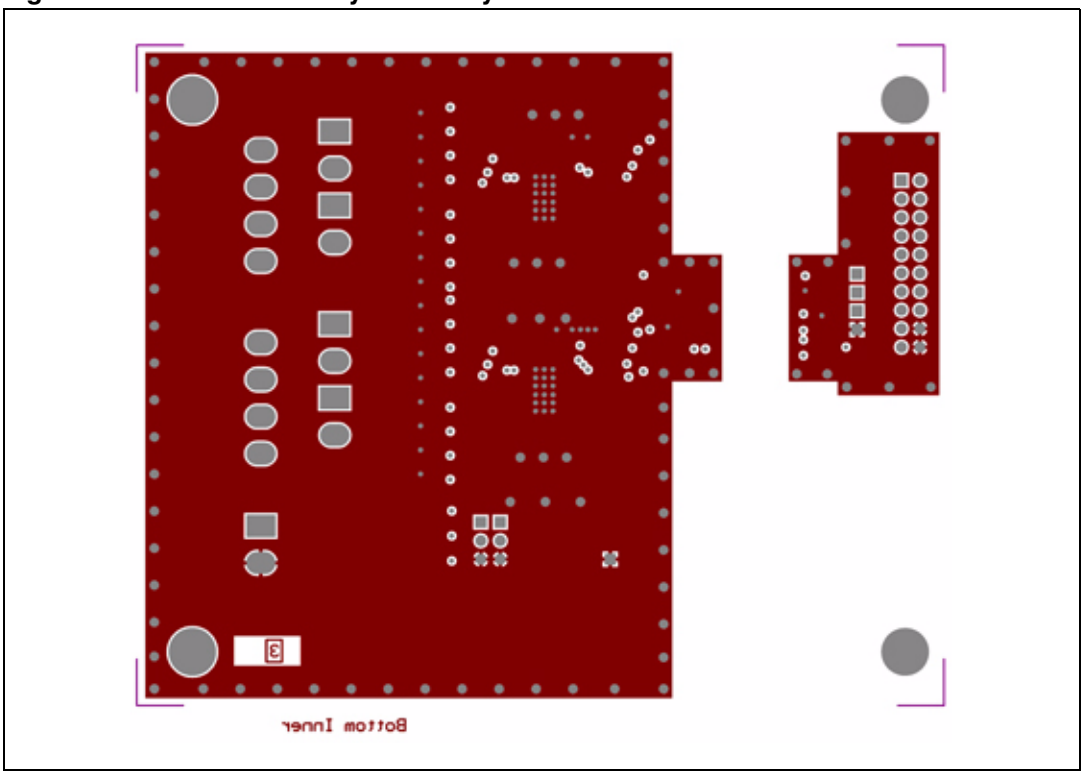


Figure 12. Bottom layer PCB layout

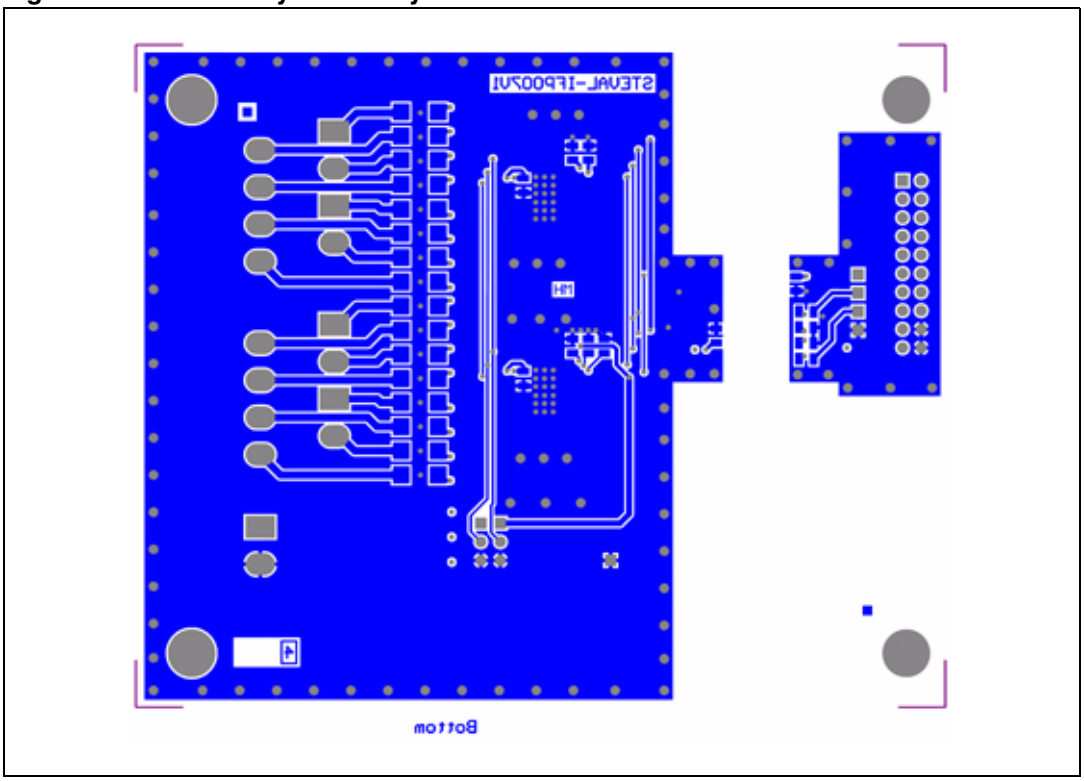


Figure 13. Top overlay PCB layout

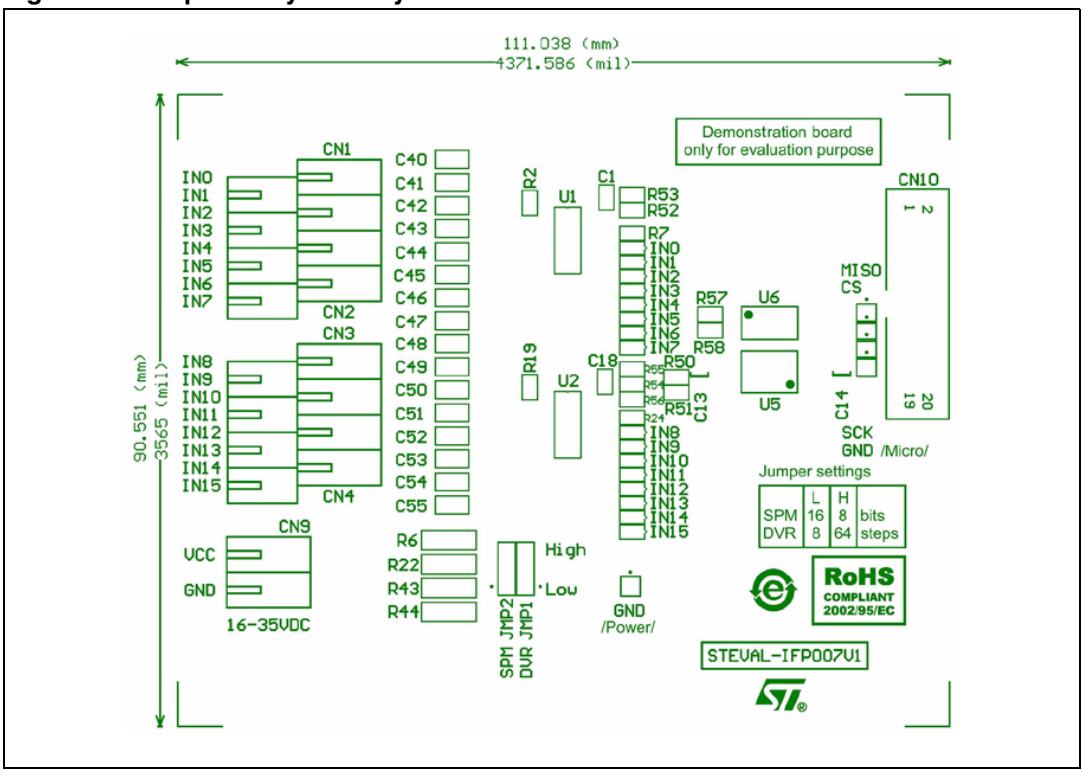
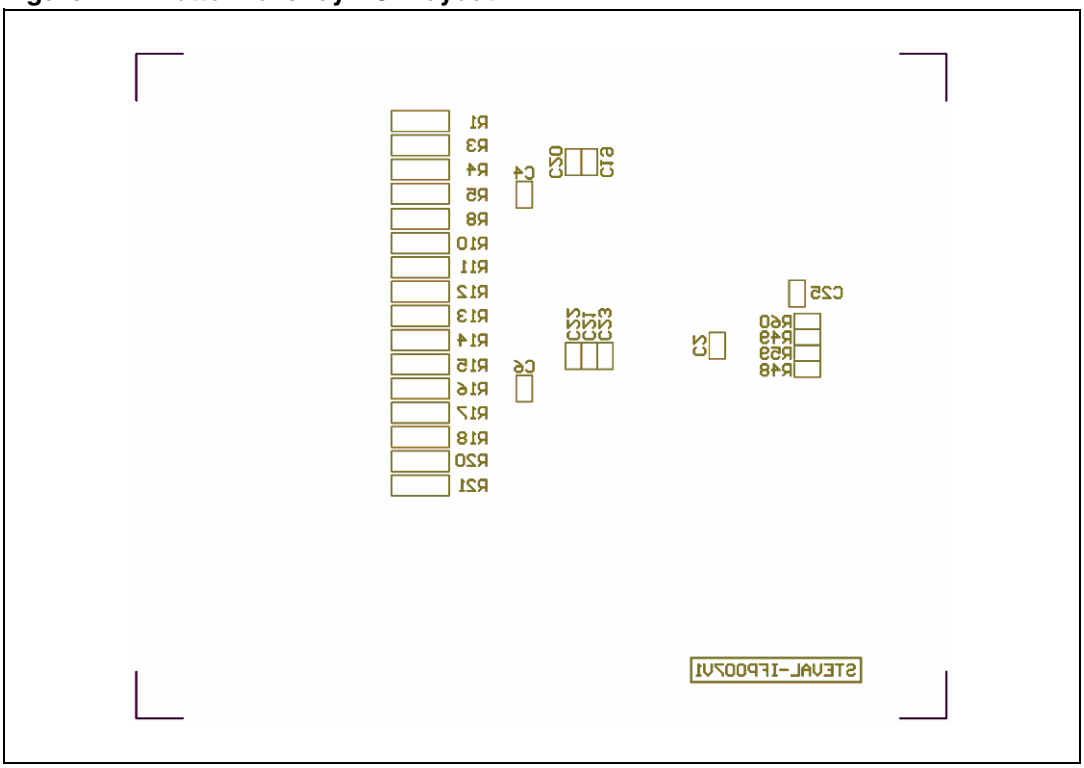


Figure 14. Bottom overlay PCB layout



4 SPI communication speed calculation

The chips are connected in cascade (daisy chain) decoupled from the control unit by high-speed low power optocouplers. SPI signals are filtered by RC cells (Rf = 220, Cf = 100 pF) placed close to each SCLT3-8BT8 and microcontroller SPI inputs. The signal filtering implementation reduces the communication bandwidth of the SPI bus.

Using the following simple equations, we can estimate the upper limit of the communication frequency:

Equation 1

$$\frac{T_{CLKMIN}}{2} - t_{su} = t_{ptot}$$

then

Equation 2

$$T_{CLKMIN} = 2 \times (t_{ptot} + t_{su})$$

and

Equation 3

$$f_{CLKMAX} = \frac{1}{T_{CLKMIN}}$$

where: t_{su} is the data setup time of the microcontroller
(for ST 32-bit microcontrollers like the STM32x, it is 5 ns)

t_{ptot} is the total propagation delay which is a sum of the propagation delays on the SPI - CLK and MISO lines and write out propagation time (influenced by the galvanic isolator, RC filtering cells and SCLT3-8BT8 chip)

The total propagation delay measured on the application is visible in the figure below; its value is approximately 160 ns. The maximum communication frequency, considering t_{su} (data setup time of an SPI master) as 5 ns, is then:

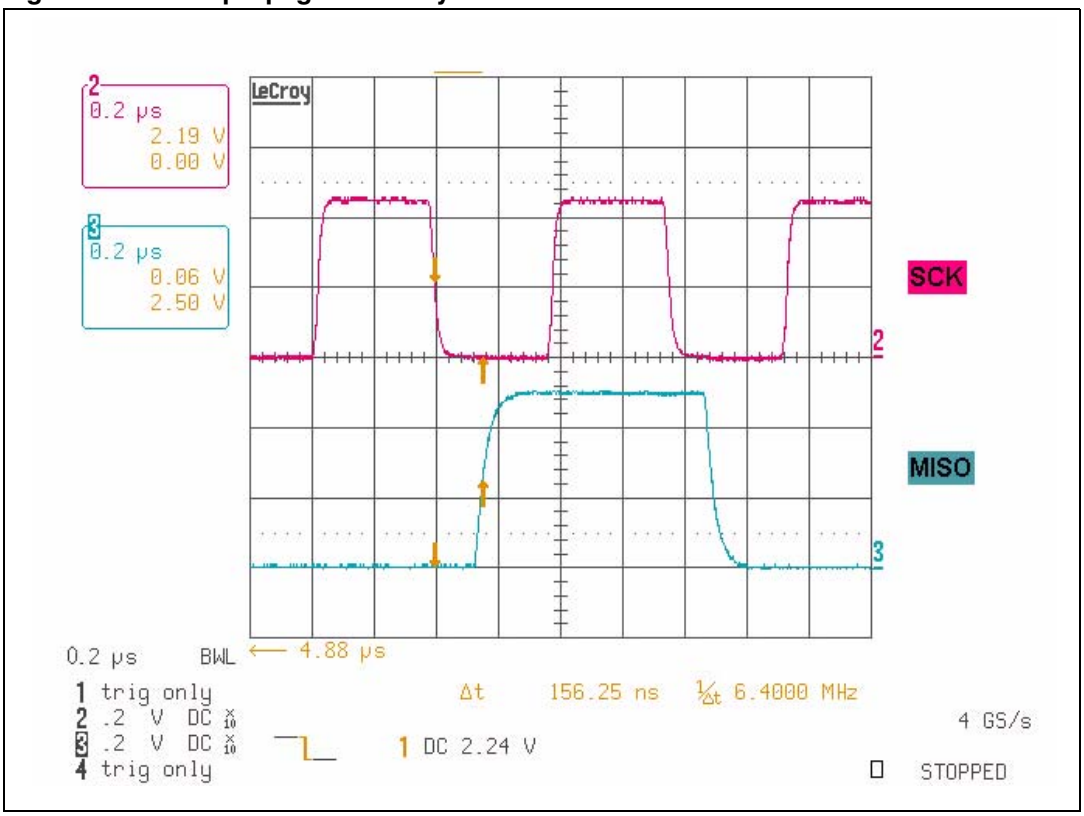
Equation 4

$$T_{CLKMIN-application} = 2 \times (t_{ptot} + t_{su}) = 2 \times (160ns + 5ns) = 330ns$$

Equation 5

$$f_{CLKMAX-application} = \frac{1}{T_{CLKMIN}} = \frac{1}{330ns} \cong 3MHz$$

Figure 15. Total propagation delay waveform



1. Red: clock signal measured on the microcontroller.
2. Blue: MISO data measured on the microcontroller.

5 Thermal management

The SCLT3-8BT8 device limits the current that flows in each input pin. Together with a voltage drop on each input pin versus GND, it also creates power dissipation. Another contribution is power dissipation coming from the supply voltage pin. The sum of both of these portions causes an increase in the junction temperature. The maximum allowed junction temperature of the SCLT3-8BT8 is 150 °C. The HTSSOP38 package with a given PCB surface has a thermal resistance (junction-to-ambient) of 80 °C / W, as specified in the device datasheet. This parameter allows the determination of the maximum ambient temperature during device operation. The ambient temperature to take into account is the air temperature near the component.

The main equation corresponds to the following:

Equation 6

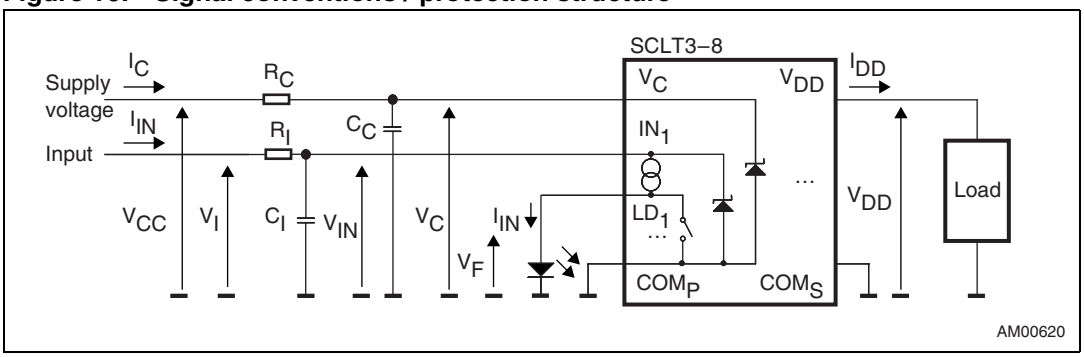
$$\Delta T_{J\text{-}A} = T_J - T_A = P_D R_{thJA}$$

where:

- T_J is the junction temperature,
- T_A is the ambient temperature,
- P_D: is the power dissipation,
- R_{thJA} is the thermal resistance junction-ambient.

This paragraph presents the method to evaluate the dissipated power.

Figure 16. Signal conventions / protection structure



The maximum ambient temperature determines the maximum allowed $\Delta T_{J\text{-}A}$. To estimate the maximum power dissipation, refer to the parameter of the datasheet that gives the maximum specification of the current limitation. The purpose is to add all “thermal supplies” inside the die. There are 2 main sources of power dissipation: the current limiters embedded in each line of the SCLT3-8BT8 device and the current consumption of the V_C pin (I_C). Current consumption of the V_C pin depends on the load of the embedded linear voltage regulator. Then, the maximum power dissipation can be estimated as follows:

Equation 7

$$P = 8 \times [(V_{IN} - V_F) \times I_{IN}] + V_C \times I_C - V_{DD} \times I_{DD}$$

As shown in *Equation 7* we must subtract the power dissipated by the indicator LEDs and voltage regulator load.

Considering the above application structure and the following conditions:

- V_{CC} = 30 V
- V_{I_MAX} = 30 V
- I_{IN_MAX} = 2.7 mA
- V_{IN_MAX} = 24 V
- f_{CLK} = 1.3 MHz
- I_C = 6 mA
- V_C = 24 V
- V_F = 1.9 V
- V_{DD} = 5 V
- I_D = 4.5 mA
- R_C = 1 kΩ
- R_I = 2.2 kΩ

the overall chip power dissipation is:

Equation 8

$$P_D = 8 \times [(V_{IN} - V_F) \times I_{IN}] + V_C \times I_C - V_{DD} \times I_{DD} = 8 \times [(24V - 1.9V) \times 2.7mA] + 24V \times 6mA - 5V \times 4.5\ A = 599mW$$

In case of a maximum allowed ambient temperature equal to 100 °C, the thermal resistance must be lower than:

Equation 9

$$R_{THJAMAX} = \frac{\Delta T_{J-A}}{P_D} = \frac{150°C - 100°C}{0.599W} = 83°C/W$$

Since the application R_{TH} value of the HTSSOP38 is 80 °C/W, the SCLT3-8BT8 works correctly at this ambient temperature.

In the final application we must consider other cases also. One example is spurious connection of one channel to negative voltage.

In this negative biasing of the input, the current (I_{REV}) flows through the protection diode. The voltage (V_{REV}) is then equal to the forward voltage of the protection diode, which is approximately 0.7 V at 16 mA.

All of the other inputs work correctly.

The total power dissipation in this case can be calculated by with the equation:

Equation 10

$$I_{REV} = \frac{V_{CC} - V_{REV}}{R_{IN}} = \frac{30 - 0.7V}{2200\Omega} = 13mA$$

and

Equation 11

$$P = 7 \times [(V_{IN} - V_F) \times I_{IN}] + V_C \times I_C - V_{DD} \times I_{DD} + V_{REV} \times I_{REV} = 7 \times [(24\ V\text{-}1.9\ V) \times 2.7\ mA] + 24\ V \times 6\ mA - 5\ V \times 4.5\ mA + 0.7\ V \times 13\ mA = 548\ mW$$

If we consider the same conditions as those above, maximum ambient temperature of 100 °C, we must achieve a thermal resistance lower than 91 °C / W. The SCLT3-8BT8 works correctly at these conditions. Connecting the input in reverse polarity conditions, the total power dissipation decreases. It allows biasing of all the SCLT3-8BT8 inputs by reverse polarity current without risk of component damage.

Special care must be taken on the serial resistor ratings. During normal operation/worst-case conditions, the power ratings of the serial resistors are:

- 16 mW for input serial resistors (R_{IN})
- 36 mW for supply serial resistor (R_C)

During a reverse polarity connection at 25 °C, the resistors must be able to dissipate:

372 mW - input serial resistors (R_{IN})

858 mW - supply serial resistor (R_C)

To increase the reliability of the resistors, considering long-term reverse polarity, the following options are suggested:

1. Parallel connection of two (or more) resistors
2. Use of high power-rating resistors
3. Reverse polarity diode connection in series with R_C resistor

At point 3 above, it is important to either choose the diode with a V_R rating higher than the required surge immunity voltage (e.g. 1 or 2 kV), or to use additional Transil™ protection (bidirectional) at the application supply voltage terminal (e.g. SM15T36CA).

6 EMC requirements

6.1 Procedure to evaluate the robustness of the SCLT3-8BT8

The reference for evaluating the robustness of the SCLT3-8BT8 device is the IEC 61131-2 international standard. This international standard provides all requirements and test conditions applicable to programmable logic controllers (PLCs) and their associated peripherals.

The IEC 61131-2 standard specifies the electromagnetic compatibility (EMC) requirements and the nature of the tests to perform in to determine if the system meets these requirements. The levels of each test depend on the zone where the system will be installed. The most typical industrial environmental levels correspond to zone B: local power distribution zone and dedicated power distribution zone (see table 28: “EMC immunity zones” of the IEC 61131-2-Ed2 standard). The following paragraphs recall the test levels for this zone.

6.2 ESD tests (according to IEC 61000-4-2)

The electrostatic discharge test shall be applied to operator accessible devices. This means that these tests have to be performed on each connector pin. The required levels are: air discharge: ±8 kV contact discharge: ±4 kV.

The PLC system shall continue to operate as intended. Temporary degradation of the performance is acceptable during the test, but the system must recover by itself after the test (criteria “B” according to the IEC61131-2 standard).

6.3 Burst tests (according to IEC 61000-4-4)

The fast transient burst tests must be applied on all input pins of the system. A capacitive clamp-coupling device (50-200 pF) must be used as described in the IEC 61000-4-4 standard. The required burst voltage levels are: analog or DC I/O: ±1 kV, DC power line: ±2 kV. The PLC system shall continue to operate as intended. Temporary degradation of the performance is acceptable during the test, but the system must recover by itself after the test (criteria “B” according to the IEC 61131-2 standard).

6.4 Surge test (according to IEC 61000-4-5)

Since the voltage surge consists of a single but energetic pulse, the SCLT3-8BT8 device embeds an overvoltage protection on each point. The absorbed energy complies at least with the requirements of the IEC 61131-2 standard. The high energy surge test must be applied on all input pins of the system. For all analog inputs, the coupling method is a 42 Ω serial resistor and a 0.5 µF capacitor. For DC power line, the coupling is 2 Ω, 18 µF with differential mode, and 12 Ω, 9 µF with common mode. The required voltage surge levels are: analog or DC I/O: 0.5 kV (line-to-line and line-to-earth coupling modes), DC power line: 0.5 kV (line-to-line), DC power line: 1 kV (line-to-earth). The PLC system shall continue to operate as intended. Temporary degradation of the performance is acceptable during the test, but the system must recover by itself after the test (criteria “B” according to the IEC 61131-2 standard).

6.5 Conducted disturbance tests (according to the IEC 61000-4-6)

The conducted radio frequency interference test must be applied on all input pins of the system. The frequency range is 150 kHz to 80 MHz, with 80% amplitude modulation of a 1 kHz sinusoidal wave. A CDN (coupling/decoupling network) or a current coupling clamp (as described in the IEC 61000-4-6 standard) must be used to apply stress to the system. The required level is: 3 V_{RMS}, whatever the tested system input is. The PLC system shall continue to operate as intended. No loss of function or performance is acceptable (criteria “A” according to the IEC 61131-2 standard).

6.6 Reverse analog input polarity tests

The test procedure is described in the IEC 61131-2 standard (paragraph 5.4.4.5 of Ed2 of the standard). A signal of reverse polarity (negative voltage) for unipolar analog inputs is applied for 10s. The result of this test shall be as stated by the manufacturer. Each input of the SCLT3-8BT8 device may be biased to a reverse polarity. This case corresponds to a connection mistake, or a reverse biasing that is generated by the demagnetization of a monitored inductive solenoid. The input involved withstands the high reverse current up to 20 mA; its corresponding bit in the data frame remains in a logic low state. The other inputs remain operational. Considering the supply operation, a reverse blocking diode can be connected between the module ground and the common COM pin to protect the application (especially the serial resistors) from a spurious reverse supply connection. The thermal management of this accidental situation is described in *Section 4: SPI communication speed calculation*.

7 EMC testing

The EMC requirements according to the IEC 61131-2 standard have been verified. Application tests show much better results than given by the industrial standard. Test requirements and results are listed in the table below. No additional protection devices have been used in the application.

Table 2. EMC immunity test requirements and results

	Minimum requirements of international standards			Robustness of the STEVAL-IFP007V1			
	Tests conditions		Levels	Tests conditions		Levels	Behavior of the SCLT3-8BT8
ESD test IEC61000-4-2	Air discharge		±8 kV	R_C = 1 kΩ R_{IN} = 2.2 kΩ		±8 kV	
	Contact discharge		±4 kV	R_C = 1 kΩ R_{IN} = 2.2 kΩ		±6 kV	
Burst test IEC61000-4-4	Analog input		±1 kV	R_{IN} = 2.2 kΩ	C_{IN} = 1 nF C_C = 33 nF	±4 kV ±6 kV(1) ±8 kV (1),(2)	No failure, no disturbance
	DC power line		±2 kV	R_C = 1 kΩ			
				SPI signals R-C filter: 220 Ω - 100 pF			
Surge test IEC61000-4-5	Analog input	42 Ω, 0.5 µF differential and common mode	±0.5 kV	Analog input	R_{IN} = 2.2 kΩ	±2 kV	No failure, temporary disturbance
	DC power line	2 Ω, 18 µF differential mode	±0.5 kV	DC power line	R_C = 1 kΩ	±2 kV	
		12 Ω, 9 µF common mode	±1 kV			±2 kV	
Conducted disturbance test IEC61000-4-6	150 kHz to 80 MHz	22 nF capacitors at the output	3 V_{RMS} AM ± 80%	150 kHz to 80 MHz	R_{IN} = 2.2 kΩ C_{IN} = 1 nF at the INPUT	10 V_{RMS} AM ± 80%	No failure, no disturbance
Reverse input polarity test	$-V_{CC}$ applied to one input during 10 s			–30 V_{DC} applied to one input, +30 V_{DC} on the others			No failure, no cross-talk

1. Primary and secondary grounds of the optocouplers have been coupled with a 10 pF capacitor
2. Forced input filtering capacitors to maximize EFT immunity (C40 - C55 = 22 nF) with a drawback of bandwidth reduction (<10 kHz).

8 Ordering information

The demonstration board is available through the standard ordering system, with order code STEVAL-IFP007V1. The complete kit contains:

- Demonstration board, assembled as described in *Section 2.2*
- Demonstration board documentation
- PCB fabrication data, such as gerber files
- Assembly files (pick-and-place)
- Component documentation

9 Conclusion

This document illustrates that the SCLT3-8BT8 application works in harsh environments without problems. All industrial standard requirements are fulfilled. Moreover, the test levels are higher than required for a majority of final products. No additional protection devices are necessary, increasing the cost-effectiveness of the application.

The SCLT3-8BT8 application passed the reverse polarity tests, including the thermal management considerations.

10 References

1. SCLT3-8BT8 device datasheet
2. IEC 61131-2 - Programmable Controllers - Equipment Requirements and Tests
3. EN 60947-5-2: Low-voltage switchgear and controlgear - Part 5-2: Control circuit devices and switching elements - Proximity switches
4. IEC 61000-4-2: Electrostatic discharge
5. IEC 61000-4-4: Electrical fast transient/burst immunity test
6. IEC 61000-4-5: Surge immunity test
7. IEC 61000-4-6: Immunity to conducted disturbances, induced by radio-frequency fields.

11 Revision history

Table 3. Document revision history

Date	Revision	Changes
06-Oct-2009	1	Initial release.